AN10954

GreenChip SR TEA1795T dual synchronous rectification driver IC

Rev. 1 — 14 December 2010

Application note

Revision history

Rev	Date	Description
v.1	20101214	First issue

Contact information

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1. Introduction

The TEA1795T is a dual synchronous rectifier driver IC for a resonant converter. Using this IC the gates of two separated MOSFETs, configured as diodes on the secondary side of a resonant converter, can be controlled. Figure 1 shows the basic configuration of a resonant converter with two SR MOSFETs on the secondary side. The MOSFETs are placed in the ground path of the circuit, making the supply of the driver IC easier.
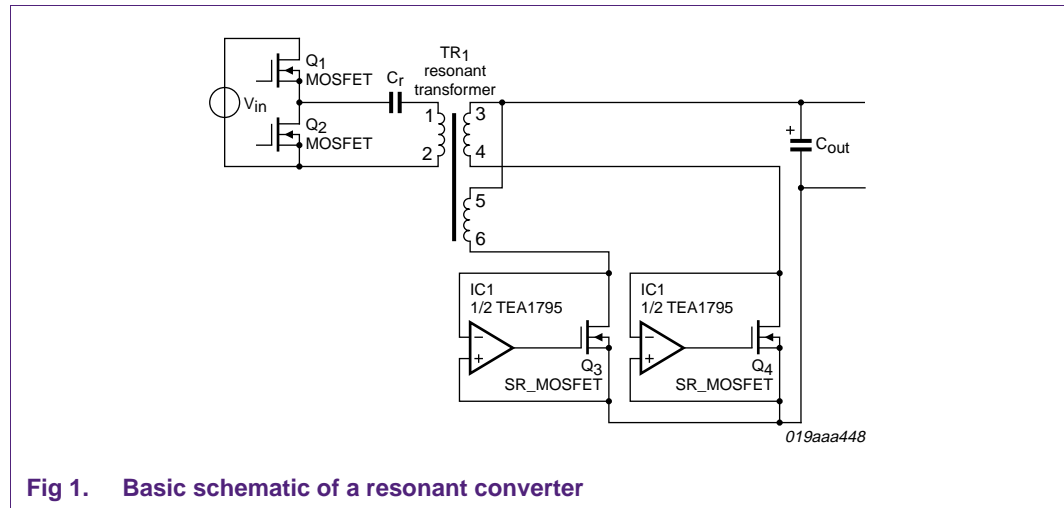

Fig 1. Basic schematic of a resonant converter

2. Quick start-up

This section describes how to start the device quickly. The IC is suitable in a resonant converter and can drive two SR MOSFETs on secondary side (see Figure 1). The MOSFETs have to be placed with their source at ground level. The IC can drive two MOSFETS independently because there are two drivers in the package.

The drain-source voltage (V_{DS}) is measured separately for each driver to determine what the status of the MOSFET should be (on or off). When a negative current is flowing through the MOSFET or, in other words, the anti-parallel diode is conducting, the MOSFET is turned on. The negative current is detected by a voltage drop over the MOSFET of at least −0.6 V. A comparator with a threshold level of −220 mV becomes HIGH and causes the MOSFET to turn on.

A timer is triggered, which stops the output from changing for a period of 520 ns in order to prevent any form of oscillation. After the blanking time the MOSFET can either be turned off or stay turned on, depending on the value of V_{DS}.

The drain-source voltage must be higher than −12 mV for the MOSFET to turn off. After the MOSFET has been turned off a second timer is triggered and the MOSFET status does not change for a period of 400 ns. Then the MOSFET can be turned on again.

In addition to the levels of −12 mV and −220 mV, a third level is used which regulates the drain-source voltage to −25 mV. This third level is active when V_{DS} is between −25 mV and −12 mV. It was added to speed up the turn-off of the MOSFET (see Section 7.1.1).

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Figure 2 shows the pinning diagram of the TEA1795T. The DSA and SSA pins or the DSB and SSB pins must be connected to the drain and the source of the MOSFET to measure the drain-source voltage. The SSA and SSB pins must be connected as close as possible to the source pins. The DSA and DSB pins must be connected as close as possible to the drain pins. This prevents wrong measurement values being obtained because of the voltage drop over the tracks and the layout of the Printed-Circuit Board (PCB). The outputs of the drivers are pins GDA and GDB, which have to be connected to the gates of the MOSFETs.

The supply pin of the IC is V_{CC}. It can be connected to an output voltage of the resonant converter because of its wide supply voltage range (8.5 V to 38 V).
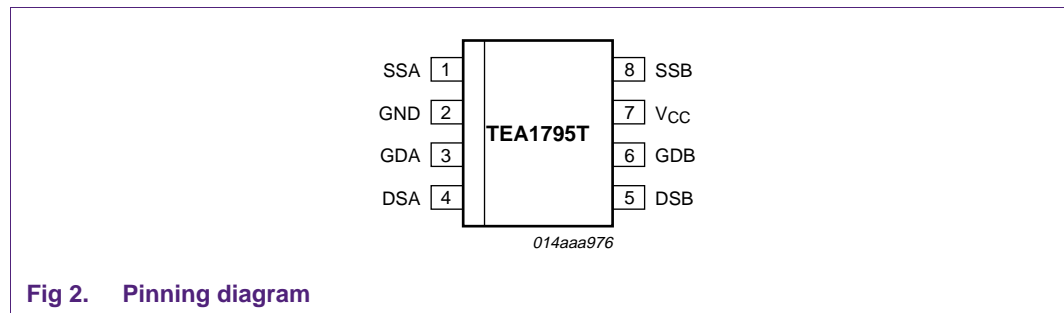
```
        SSA  1          8  SSB
        GND  2          7  VCC
             TEA1795T
        GDA  3          6  GDB
        DSA  4          5  DSB
              014aaa976
```

Fig 2. **Pinning diagram**

Table 1. **Pin descriptions**

Symbol	Pin	Description
SSA	1	source sense input MOSFET A
GND	2	ground
GDA	3	gate driver output MOSFET A
DSA	4	drain sense input for synchronous timing MOSFET A
DSB	5	drain sense input for synchronous timing MOSFET B
GDB	6	gate driver output MOSFET B
V_{CC}	7	supply voltage
SSB	8	source sense input MOSFET B

Careful attention must be paid to the layout of the PCB to get the best possible results. Tracks from drain to DSA (or DSB) and from source to SSA (or SSB) form a loop which must be as short as possible. This can be achieved by routing them as closely as possible and parallel to each other. Alternatively, they can be put above each other in a dual-layer PCB (see Figure 23). A filter can be added to the system to improve the design, depending on the MOSFET used and the mode of operation (CCM or DCM) (see Section 7.1.2 and Section 7.2.1).

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3. Resonant converter versus flyback

The TEA1795T has been developed for a resonant converter supply. It is derived from the TEA1761, a MOSFET driver IC for flyback SR. The main difference is the blanking time after turn-on.

The differences between a resonant converter supply and a flyback supply are:

- The secondary current does not have to start at the beginning of a primary switching transition
- The current increases and decreases (sinusoidally)
- The switching frequency can be much higher
- The dI/dt of the current is much higher

In a flyback converter the secondary phase starts when the current through the switch (diode, MOSFET) is at its maximum. This is not the case in a resonant converter, where the current starts at 0 A and rises until it has reached its maximum. Then it decreases again. The overall shape of the current is more or less sinusoidal (see Figure 3).
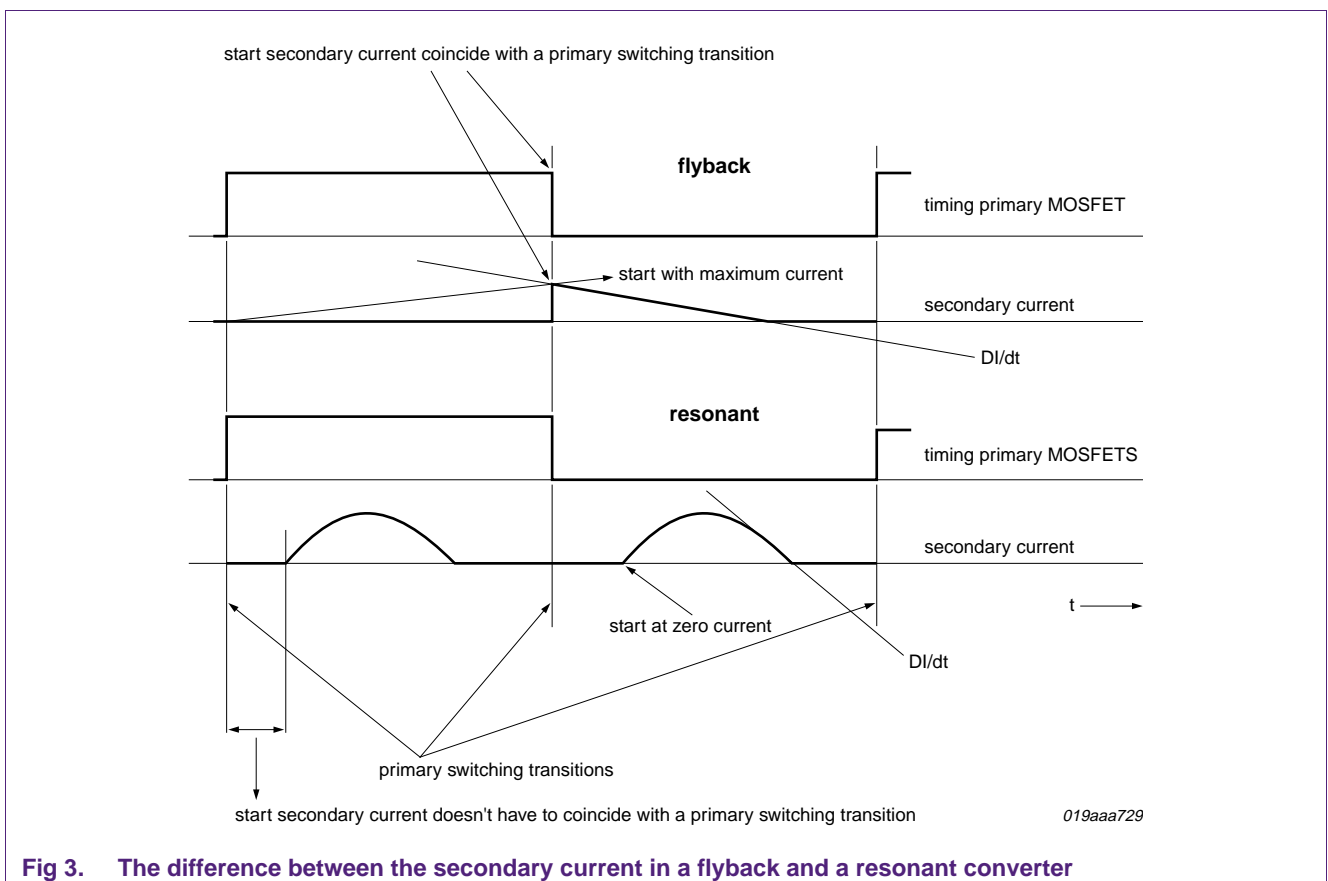

Fig 3. **The difference between the secondary current in a flyback and a resonant converter**

The current does not have to start at the beginning of a primary switching transition. This makes the timing more vulnerable to incorrect sensing, causing the SR-MOSFET to switch at the wrong moment.

4. Diodes as rectifiers

In older designs, Schottky diodes were used to rectify the current on the secondary side. The advantages of Schottky diodes compared to PN-diodes are:

- Lower voltage drop
- Less reverse recovery

The Schottky diodes also have a few disadvantages:

- Higher parasitic capacitance
- Reverse leakage current
- Not available for higher output voltages

Two modes can be distinguished in a resonant converter:

- Continuous Conduction Mode (CCM)
- Discontinuous Conduction Mode (DCM)

For DCM the secondary current can be modeled using Equation 1:

$$
\begin{cases}
I_{sec} = I_{amp} \times \left| sin(\omega_1 \times (t - t_{no})) \right| \wedge \dfrac{k \times \pi}{\omega_1} \leq t \leq \dfrac{(k+1) \times \pi}{\omega_1} \wedge k \in N \\[4mm]
I_{sec} = 0 \wedge \dfrac{(k+1) \times \pi}{\omega_1} \leq t \leq \dfrac{(k+1) \times \pi}{\omega_1} + t_{no}
\end{cases}
\tag{1}
$$

Where:

- I_{amp} is amplitude of the current
- ω_1 is the radial frequency
- I_{sec} is the secondary current
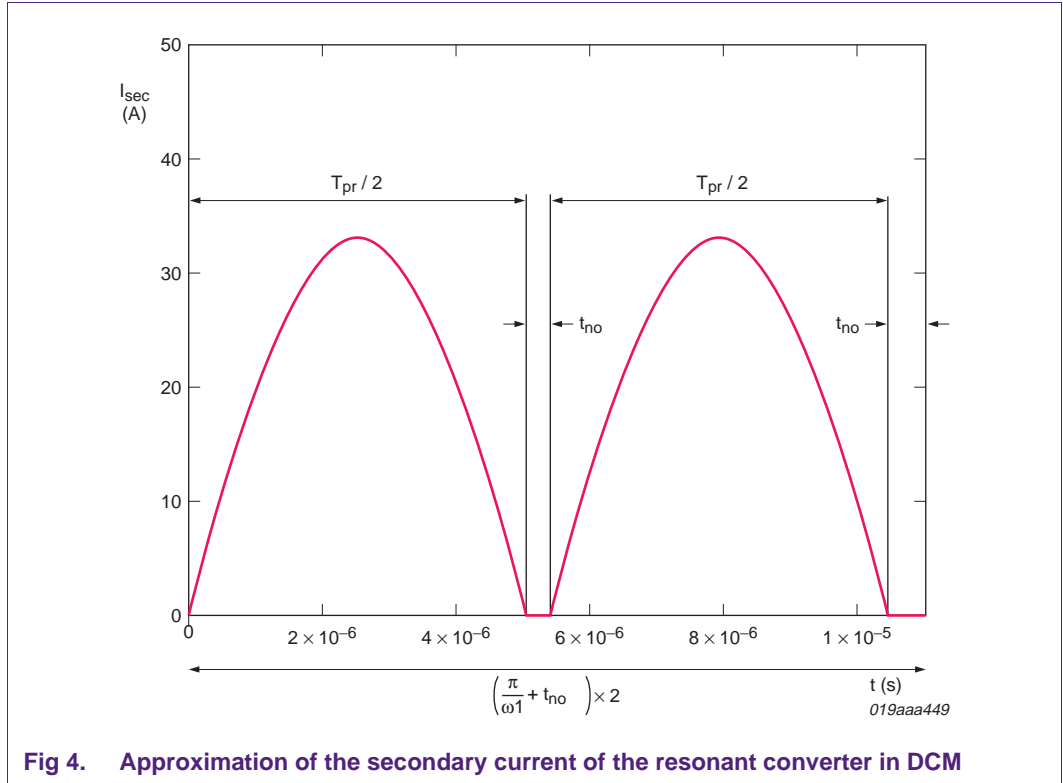- t_{no} is the time that the secondary current is zero (see Figure 4)

Fig 4. **Approximation of the secondary current of the resonant converter in DCM**

For I_{amp} Equation 2 and Equation 3 can also be written:

$$P_O = V_O \times \cfrac{1}{\cfrac{t_{pr}}{2} + t_{no}} \times \int_{0}^{\frac{t_{pr}}{2}} I_{amp} \times \sin(\omega_1 \times t)$$

$$= \frac{2}{\pi} \times V_O \times I_{amp} \times \cfrac{1}{1 + 2 \times \cfrac{t_{no}}{t_{pr}}}$$

(2)

or

$$I_{amp} = \left(1 + 2 \times \frac{t_{no}}{t_{pr}} \right) \times \frac{\pi}{2} \times \frac{P_O}{V_O}$$

(3)

Where:

- $t_{pr} = 2 \times \pi / \omega_1$
- P_O is the output power
- V_O is the output voltage

The voltage drop of a Schottky diode can be calculated with Equation 4:

$$V_f(I_d) = V_{f0} + R_d \times I_d$$

(4)

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Finally, the total dissipation in the secondary rectifiers taking the current as shown in Figure 4 can be calculated with Equation 5:

$$P_{tot} = \left(\frac{2}{\pi} \times V_F \times I_{amp} + \frac{1}{2} \times R_d \times I_{amp}^{~2} \right) \times \cfrac{1}{1 + 2 \times \cfrac{t_{no}}{t_{pr}}} \qquad (5)$$

By replacing I_{amp} with Equation 3 the power dissipation changes to Equation 6:

$$P_{tot} = \left(V_F \times \frac{P_O}{V_O} + \frac{\pi^2}{8} \times R_d \times \frac{P_O^{~2}}{V_O^{~2}} \times \left(1 + 2 \times \frac{t_{no}}{t_{pr}} \right) \right) \qquad (6)$$

Equations for the CCM case can be created as equivalents of the DCM case equations. In Section 11.2 the CCM case is presented in detail. Here only the results are shown.

Example:

- t_{no} = 500 ns
- t_{till0} = 500 ns
- P_O = 240 W
- V_O = 12 V
- R_d = 5 mΩ
- V_F = 280 mV

For CCM the dissipation in the diodes equals: 7.925 W. For DCM the dissipation equals: 8.314 W.

5. MOSFETs as rectifiers

Ideally if the diodes are replaced by SR-MOSFETs the dissipation in the DCM case is reduced to:

$$P_{tot} = \frac{1}{2} \times R_{DSon} \times I_{amp}^{~2} \times \cfrac{1}{1 + 2 \times \cfrac{t_{no}}{t_{pr}}} = \frac{\pi^2}{8} \times R_{DSon} \times \frac{P_O^{~2}}{V_O^{~2}} \times \left(1 + 2 \times \frac{t_{no}}{t_{pr}} \right) \qquad (7)$$

Example for DCM mode:

- V_F = 280 mV
- R_d = 5 mΩ
- P_O = 240 W
- t_{no} = 500 ns
- t_{pr} = 10 μs (keeping in mind that t_{pr} is not the period time but t_{pr} + 2 $\times$ t_{no} is)
- V_O = 12 V
- R_{DSon} = 4 mΩ

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With Schottky diodes, the dissipation will be 8.314 W and with MOSFETS 2.171 W. Compared to the 240 W output power this is an improvement of approximately 2.6 % (going from 3.5 % to 0.91 %). For CCM mode with t_{till0} = 500 ns and t_{sw} = 10 μs, the values are respectively 7.925 W (3.3 %) and 1.86 W (0.78 %). This is an improvement of 2.5 %.

Remark: An additional control IC is needed to turn on and turn off the MOSFET at the right time (see Section 6).

Remark: When the MOSFET is not conducting, it behaves like a diode, so losses are higher (see Equation 28).

6. Basic functionality of the TEA1795T

When using MOSFETs instead of diodes, the MOSFET has to be turned on when current is flowing through it. It has to be turned off when there is no current flowing through it. The TEA1795T IC has been developed to realize these functions. Section 6.1 describes the turn-on function. Section 6.2 describes the turn-off function.

6.1 The turn-on function

It is easy to detect if current is flowing through the MOSFET. A MOSFET that is not conducting (turned on) behaves like a diode. When current is flowing through the diode the voltage drop is above 0.5 V. A level of −220 mV has been built in in the IC to which this voltage can be compared. When this level is exceeded the TEA1795 charges the gate of the MOSFET and turns it on. Depending on the current flowing through the diode, the voltage drops to $V_{DS} = I_{DS} \times R_{DSon}$.

6.2 The turn-off function

A second level has been built in to turn the MOSFET off again. When the drain-source voltage drop is less than 12 mV, meaning that the current through the MOSFET is below a certain level (see Equation 8, the MOSFET is turned off again.

$$I_{DS\_off} \leq \frac{12\ mV}{R_{DSon}}$$

(8)

Example: if the current is behaving as described in Equation 2 and R_{DSon} = 4 mΩ, then I_{DS_off} = 3 A.

Summary: The MOSFET is turned on at V_{DS} < −220 mV. The MOSFET is turned off at V_{DS} > −12 mV.

The pin connections are shown in Figure 2. The voltage drop over the MOSFET is measured differentially (driver A: DSA (pin 4) − SSA (pin 1); driver B DSB (pin 5) − SSB (pin 8)). The outputs of the drivers are GDA for driver A and GDB for driver B. Finally, two pins are left, the GND (pin 2) and the positive connection of the power supply (V_{CC}, pin 7). In Table 1 the pinning information is listed.

7. Improving the system

The following improvements have to do with the turn-on and turn-off moments of the MOSFETs:

- Turn-on:
  - Immediate turn-off after turn-on
  - false turn-on
  - parasitic turn-on
- Turn-off:
  - premature turn-off
 - turn-off is too late
  - false turn-off

7.1 Turn-on

7.1.1 Immediate turn-off after turn-on

A blanking time has been built in to prevent the MOSFET from turning off immediately after it has been turned on, because the drain-source voltage is still above the turn-off level (-12 mV). This blanking time is typically 520 ns. If, after 520 ns the value is above the regulation level (-25 mV) or the turn-off level, the gate is discharged until the regulation level is reached or the MOSFET is turned off.

The disadvantage of the blanking time feature is that if the current becomes zero during this blanking time it reverses and causes additional losses. If, after the blanking time, the drain-source voltage is still below the regulation level, the gate voltage is lowered until the drain-source voltage equals regulation level.

The regulation level mentioned above is added to the IC. When the input voltage is higher than this regulation level but lower than the turn-off level the IC regulates the drain-source voltage to -25 mV by controlling the gate voltage of the MOSFET. The MOSFET is normally used in its linear region, but by lowering the gate voltage to just above the threshold level the MOSFET enters its saturation region. This prevents the MOSFET turning off too late when the turn-off level is reached. To turn off the MOSFET, the gate voltage only needs to decrease slightly, instead of requiring a discharge from a high gate voltage to the threshold voltage. Figure 5 shows the decision levels of the TEA1795T.
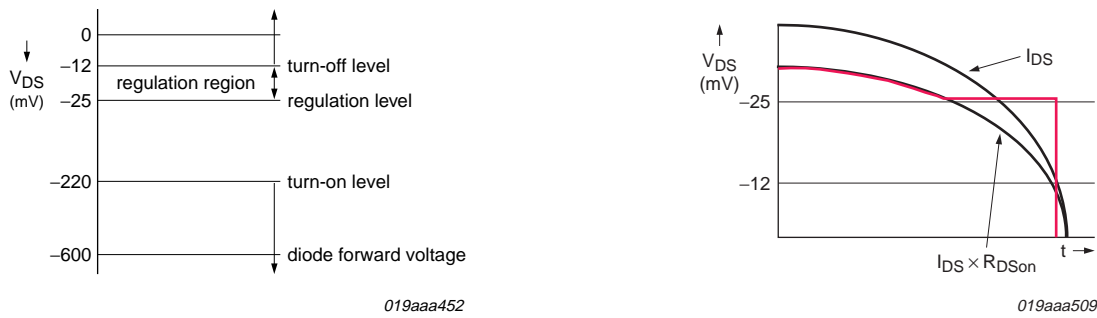
a. turn-off, regulation and turn-on levels[1]

b. Drain-source voltage[2]
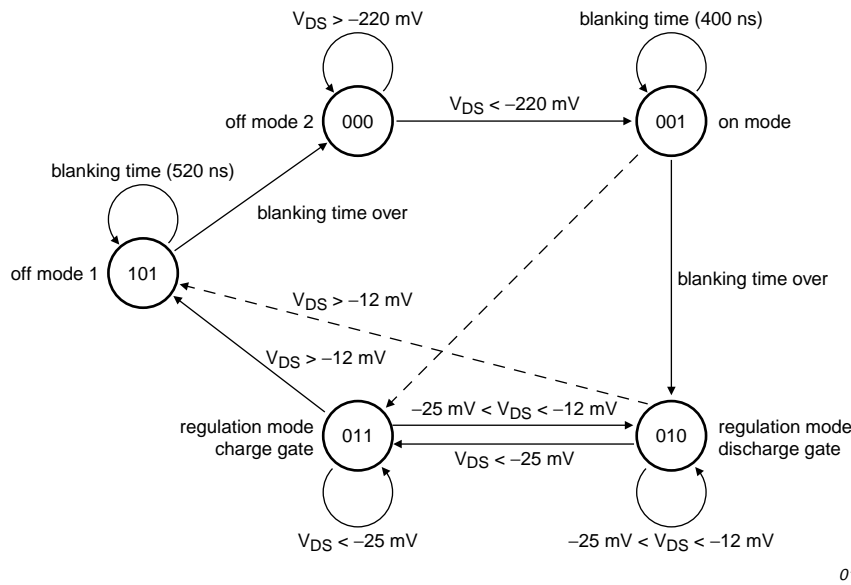
c. TEA1795T state diagram[3]

(1) Three levels are built in: turn-on level (−220 mV), turn-off level (−12 mV) and regulation level (−25 mV).

(2) If the drain-source voltage is lower than −25 mV the gate is totally charged (Linear mode). As soon as the drain-source voltage increases to above −25 mV the gate is discharged until the drain-source voltage is −25 mV again (Saturation mode). Above −12 mV the gate is fully discharged (off mode)

(3) 000, 001, 010, 011, and 101 are the five states.

Fig 5.   The decision matrix of the TEA1795

The regulation level means that between this level (−25 mV) and the turn-off level (−12 mV) the IC stabilizes V_{DS} to −25 mV by charging or discharging the gate. When the current becomes too low to keep V_{DS} at −25 mV the drain voltage exceeds −12 mV and the MOSFET is turned off very quickly. If current is still present, the MOSFET behaves like a diode again and the voltage decreases to below −0.5 V.

7.1.2 False turn-on

Ideally, the MOSFET is turned on and off at the zero crossing of the current. However, some parasitic components have a negative impact on the behavior of the synchronous rectifier. The secondary inductance and the drain-source capacitance form a resonant network which causes some oscillation of the drain-source voltage during the switching of one of the MOSFETs (primary or secondary). Figure 6 shows the schematic.
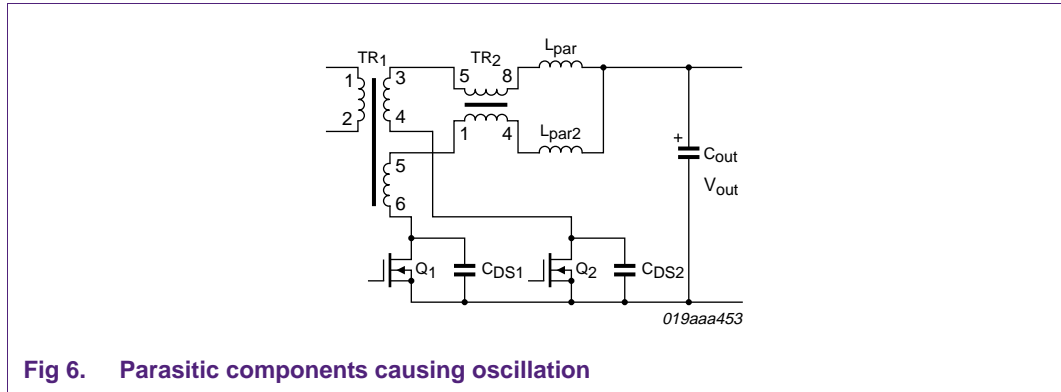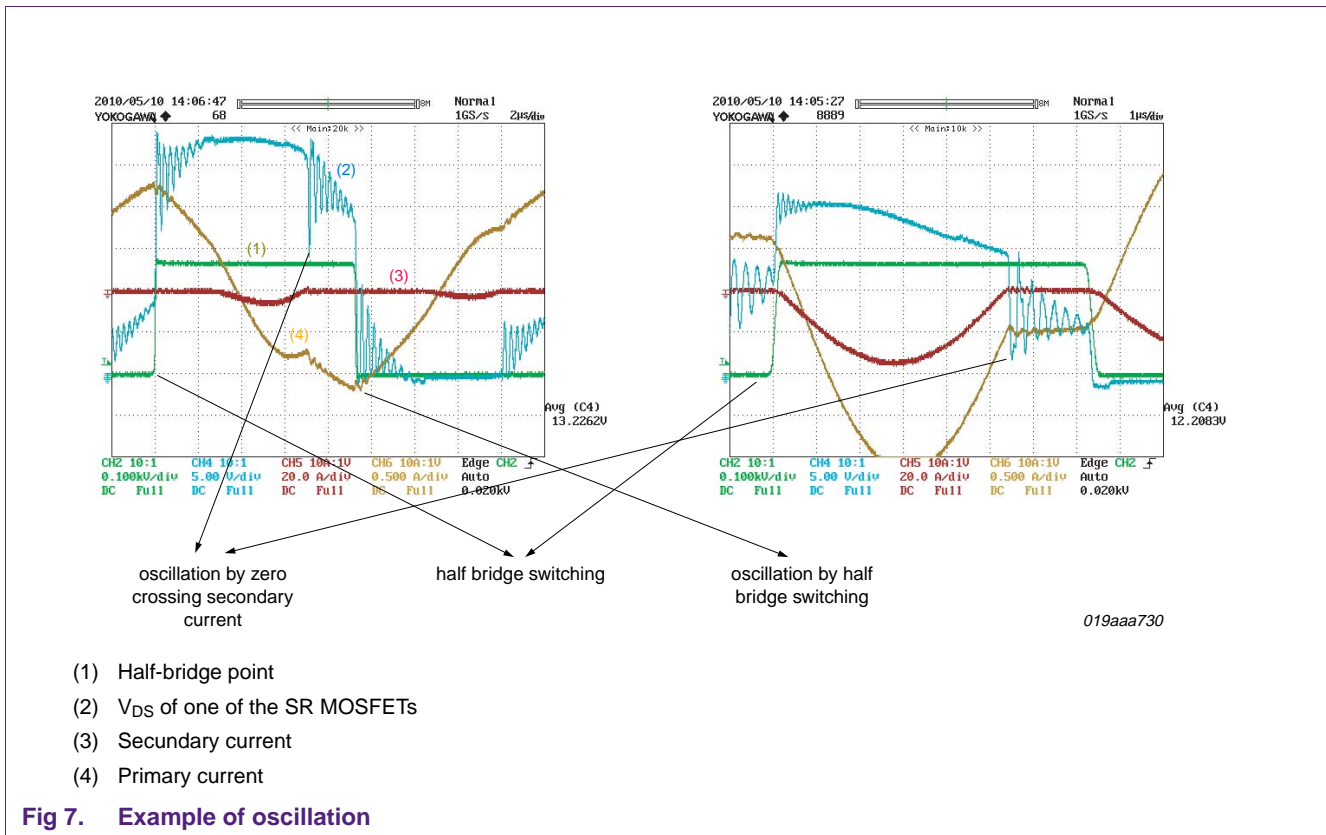

Fig 6.   Parasitic components causing oscillation

Figure 7 shows examples of oscillations. When the voltage of the drain-source decreases below −220 mV false triggering of the MOSFET occurs, causing unstable behavior.

(1) Half-bridge point
(2) V_{DS} of one of the SR MOSFETs
(3) Secondary current
(4) Primary current

Fig 7.   Example of oscillation

An RC-filter is placed in front of the input of the driver IC to filter out the high frequency component in the drain-source voltage (see Figure 11). This prevents false triggering of the MOSFET.

The voltage difference between pin 1 and pin 4 (and also between pin 5 and pin 8) for a step from V_I to 0 V can be calculated with Equation 9:

$$V_{C1}(t) = V_I \times exp\left(-\frac{t}{R \times C}\right)$$ (9)

Where:

- $V_{C1}(t)$ = 0.1 V_I (= 10 % of the end value)
- t = 100 ns
- R = 3.9 kΩ

The result is a capacitor value (C) of 10 pF.

7.1.3 Parasitic turn-on

When the drain-source voltage (Figure 8, line 3) rapidly increases, the gate voltage (Figure 8, line 1) is lifted to the threshold level of the MOSFET, causing it to turn on. This is caused by the weak sinking capability of the driver output during the transition from Regulation mode to the Off mode of the IC (see Figure 5). During the regulation mode the sinking capability is taken care by a 24 Ω MOSFET. The 1 Ω MOSFET is only available in the off-mode. It takes time to turn on this 1 Ω MOSFET, because of the internal delay. When this MOSFET is conducting, the gate of the SR MOSFET is discharged again. Therefore a spike is visible on the gate during the transition.
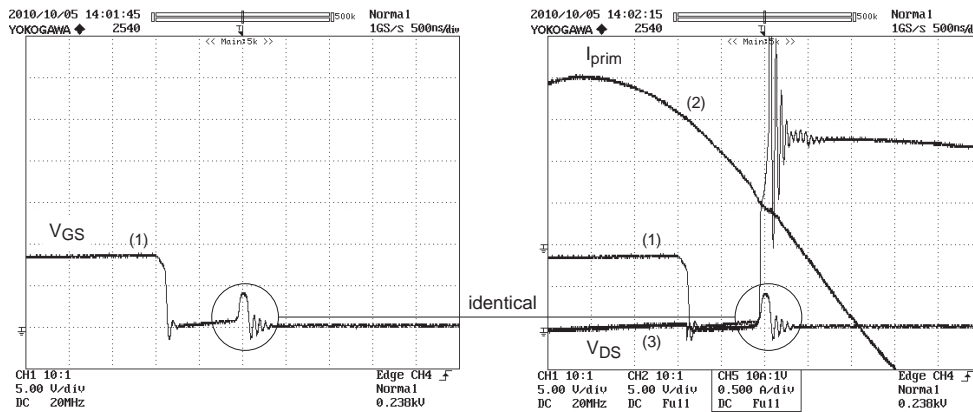
The gate voltage of one of the SR MOSFETs (left). It shows a small pulse after the MOSFET is turned off. The small pulse is caused by fast rising of the drain-source voltage (right).

(1) Gate source voltage.

(2) Primary current.

(3) Drain-source voltage over the primary MOSFET.

Fig 8. Parasitic turn-on

7.2 Turn-off

7.2.1 Premature turn-off

The drain-source voltage is measured between two points of the PCB. The impedance between these points incorporates the resistance of the track, the MOSFET and inductance L_{par}. L_{par2} is also part of the parasitic inductance, but it does not have any impact on the measurement (see Figure 9).

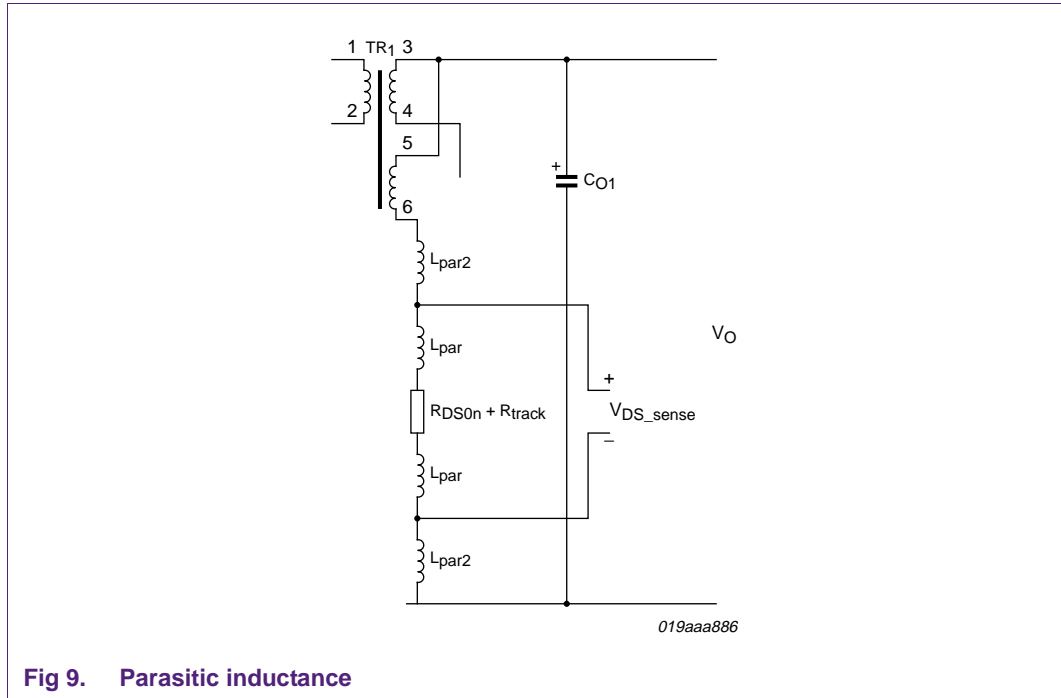**Fig 9.   Parasitic inductance**

Equation 10 calculates the voltage over the inductance:

$$V_L(t) = L_{par} \times \frac{dI_{ds}}{dt} \tag{10}$$

If the secondary current can be modeled using Equation 11:

$$I_{DS}(t) = \left| I_{amp} \times sin(\omega_1 \times t) \right| \tag{11}$$
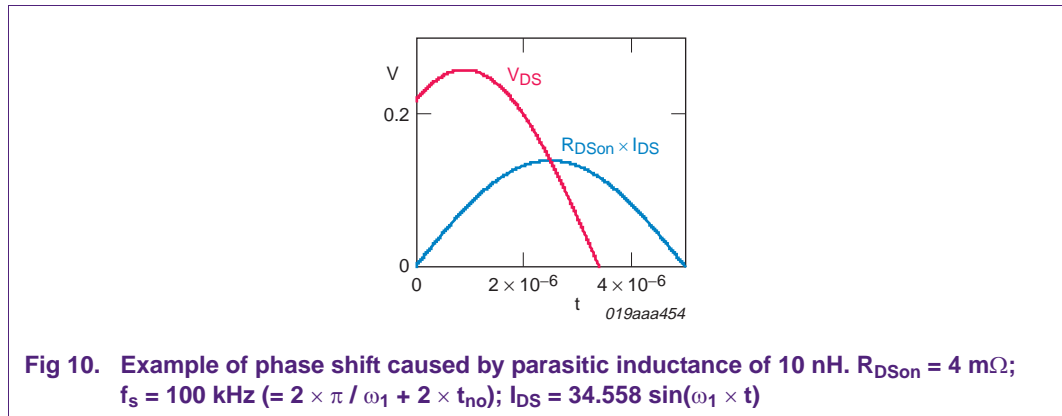
Then the induced voltage equals:

$$V_L(t) = L_{par} \times \frac{d}{dt}(I_{amp} \times sin(\omega_1 \times t)) \tag{12}$$

Combined with the resistance between the measuring points the voltage drop equals:

$$\begin{bmatrix} V_{DS}(t) = I_{amp} \times L_{par} \times \omega_1 \times cos(\omega_1 \times t) + R_{DSon} \times I_{amp} \times sin(\omega_1 \times t) \\ \qquad = I_{amp} \times \sqrt{(L_{par}^2 \times \omega_1^2 + R_{DSon}^2)} \times cos(\omega_1 \times t - \varphi) \\ \varphi = atan\left(\frac{R_{DSon}}{L_{par} \times \omega_1}\right) \end{bmatrix} \tag{13}$$

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Figure 10 shows an example, where:

- L_{par} = 10 nH
- R_{DSon} = 4 mΩ
- $I_{DS}(t)$ = 34.558 × sin(ω_1 × t)

Fig 10. Example of phase shift caused by parasitic inductance of 10 nH. R_{DSon} = 4 mΩ; f_s = 100 kHz (= 2 × π / ω_1 + 2 × t_{no}); I_{DS} = 34.558 sin(ω_1 × t)

The time (t1) of the early turn-off of the MOSFET can be calculated with Equation 14:

$$\frac{t_{pr}}{2} - t_1 = acos\left(\left(\frac{V_{th}}{I_{amp} \times \sqrt{L_{par}^2 \times \omega_1^2 + R_{DSon}^2}}\right) + \varphi\right) \tag{14}$$

In this case it is approximately 1.627 μs, giving an additional loss of 3.686 W $-$ 2.171 W = 1.515 W. The result of this inductance is that the losses are almost doubled. Therefore a solution to decrease these losses is required. One solution is to use an RC filter as a compensation network (see Figure 11).

Fig 11. RC-filter as compensation network
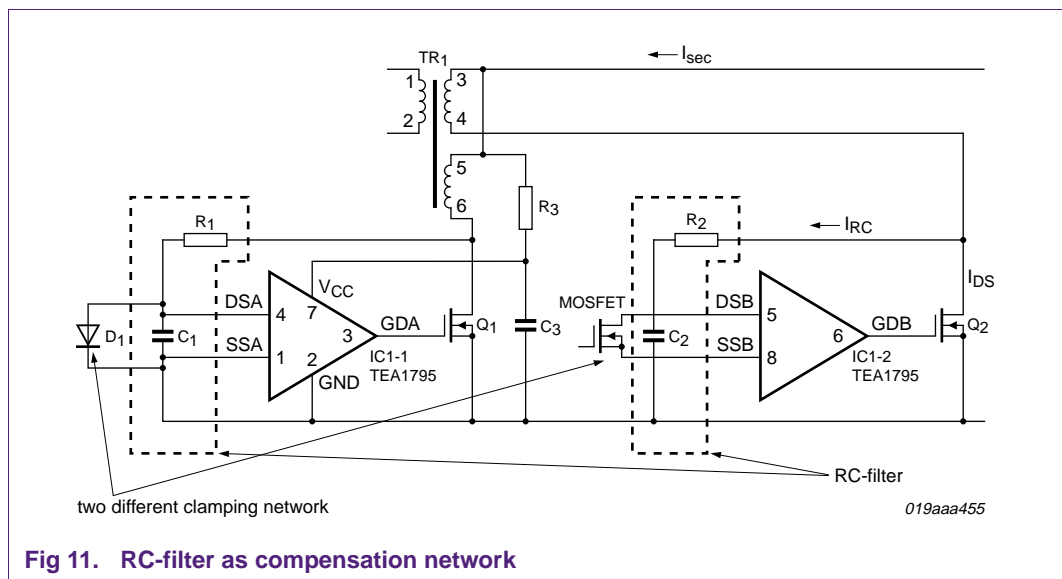
The associated equations are:

$$\begin{cases} I_{\text{sec}}(s) = I_{DS}(s) + I_{RC}(s) \\[2mm] R_1 \times I_{RC} + V_{C1} = L_{par} \times \dfrac{\mathrm{d}I_{ds}}{\mathrm{d}t} + R_{DSon} \times I_{DS} \\[2mm] I_{RC} = C_1 \times \dfrac{\mathrm{d}V_{C1}}{\mathrm{d}t} \end{cases} \tag{15}$$

The solution for this system in the time domain is given in Section 11. In the s-domain the system can be written as:

$$\begin{cases} I_{\text{sec}}(s) = I_{DS}(s) + I_{RC}(s) \approx I_{DS}(s) \\[2mm] \left(R_1 + \dfrac{1}{C_1 \times s}\right) \times I_{RC} = (s \times L_{par} \times R_{DSon} + 1) \times I_{DS} \\[2mm] V_{C1} = \dfrac{I_{RC}}{C_1 \times s} \end{cases} \Rightarrow \begin{cases} I_{\text{sec}}(s) \approx I_{DS}(s) \\[2mm] V_{C1} = \dfrac{\left(\dfrac{L_{par} \times s}{R_{DSon}} + 1\right)}{(R_1 \times C_1 \times s + 1)} \times R_{DSon} \times I_{DS} \end{cases} \tag{16}$$

If:

$$\frac{L_{par}}{R_{DSon}} = R_1 \times C_1 \tag{17}$$
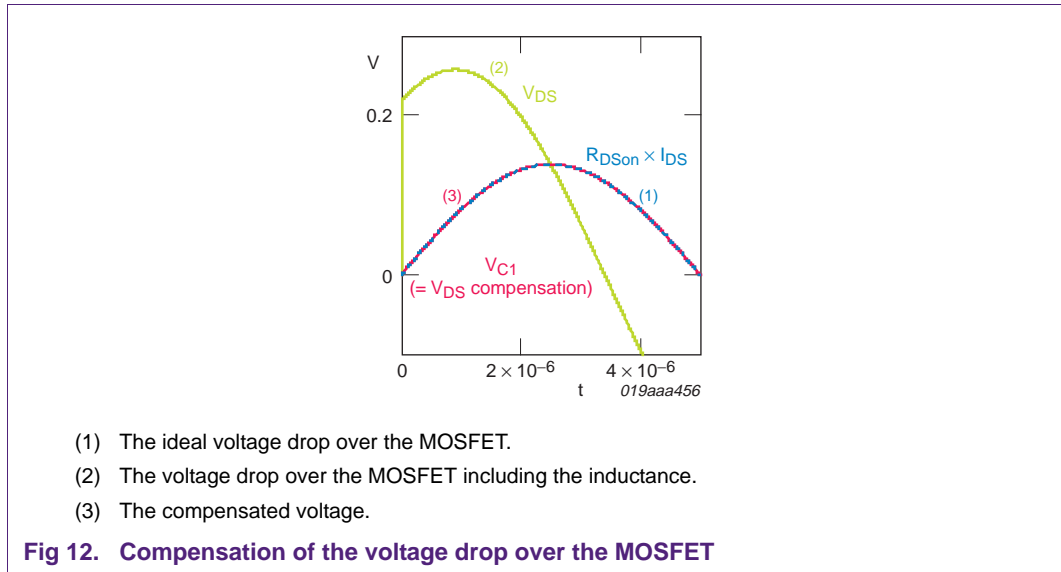
the last part of Equation 16 changes to:

$$V_{C1} = R_{DSon} \times I_{DS} \tag{18}$$

Example:

- L_{par} = 10 nH
- R_{DSon} = 4 mΩ
- R_1 = 3.9 kΩ

Results in: C_1 = 641 pF.

Figure 12 shows the result of the compensation. Ideally, the capacitor voltage follows the drain-source voltage very accurately. In reality, however, this is very often not the case.

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(1) The ideal voltage drop over the MOSFET.

(2) The voltage drop over the MOSFET including the inductance.

(3) The compensated voltage.

**Fig 12. Compensation of the voltage drop over the MOSFET**

When one of the secondary MOSFET is conducting, the other MOSFET has a voltage drop of approximately twice the output voltage. The compensation capacitor C_1 is also charged to this voltage. When the voltage drops to below zero because the voltage over the transformer reverses, the capacitor is also discharged to -220 mV. If the built-in diode of the MOSFET conducts this is approximately -0.6 V. Figure 13 shows the voltage of the capacitor as a function of time. It takes 10.3 μs to discharge the capacitor.
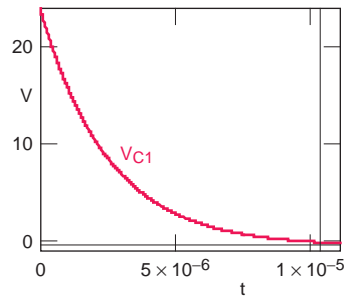
019aaa457

a. The discharge time of the compensation capacitor equals 10.3 μs. This time can also be calculated with Equation 9 (R_1 = 3.9 kΩ; C_1 = 641 pF; V_{C1} = −0.2 V, V_{in} = 24 V).
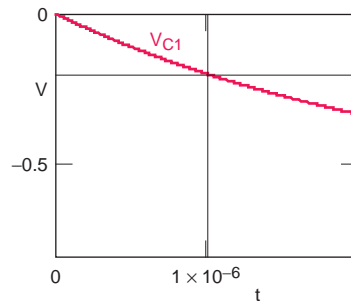
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b. The capacitor voltage is clamped down to 0 V:
The discharge time compensation capacitor equals 1.02 μs

Fig 13. The discharge time of the compensation capacitor from 24 V to −0.22 V when the MOSFET is turned on

Without further adaptations this compensation circuit does not work. The first one is to clamp the voltage to 0 V (MOSFET) or 250 mV (RF Schottky diode). This reduces the discharge time (from 0 V to −220 mV) to 1.02 μs. The second one to compromise between the delay caused by capacitor C_1 and to what extent the induction (L_{par}) is compensated, expressed by the function "Early" (see Figure 14). A larger compensation capacitor results in a larger turn-on delay, which again results in a better compensation.
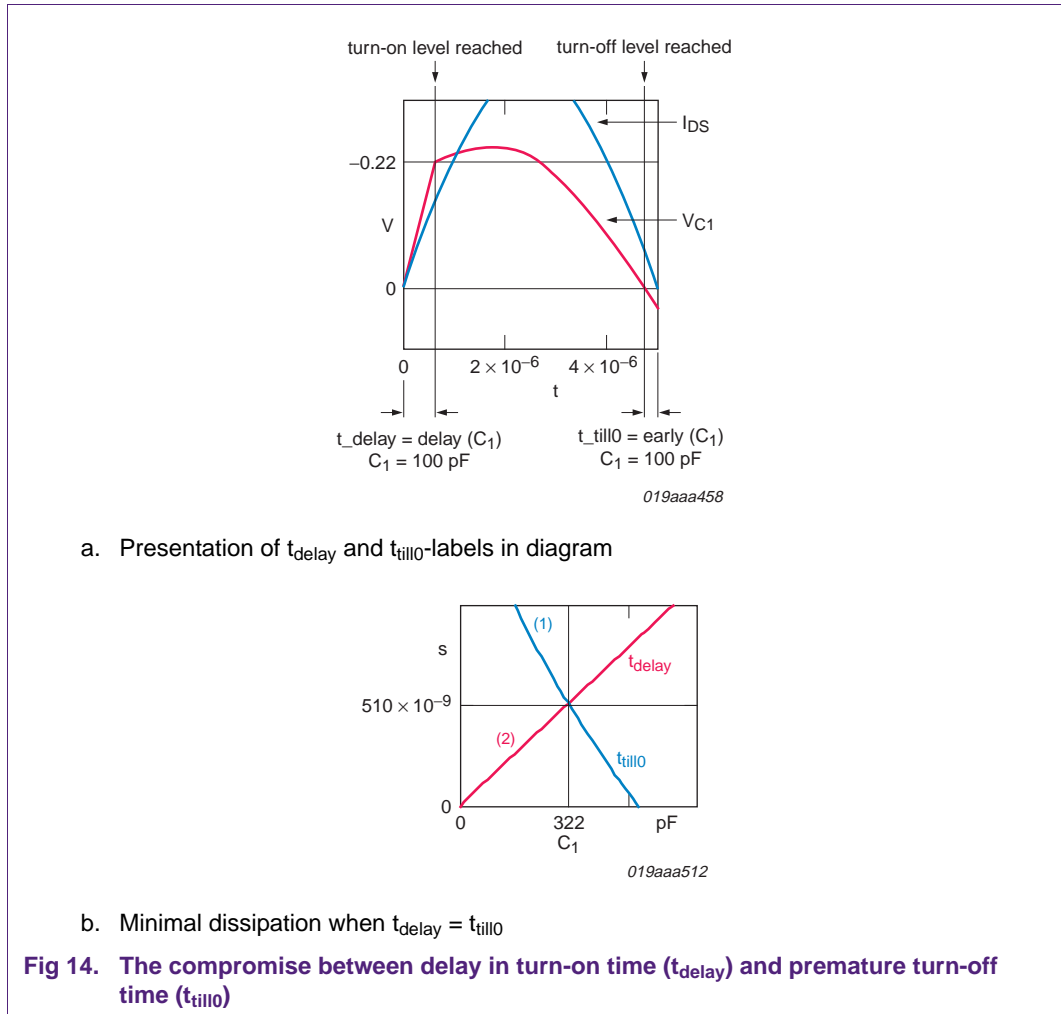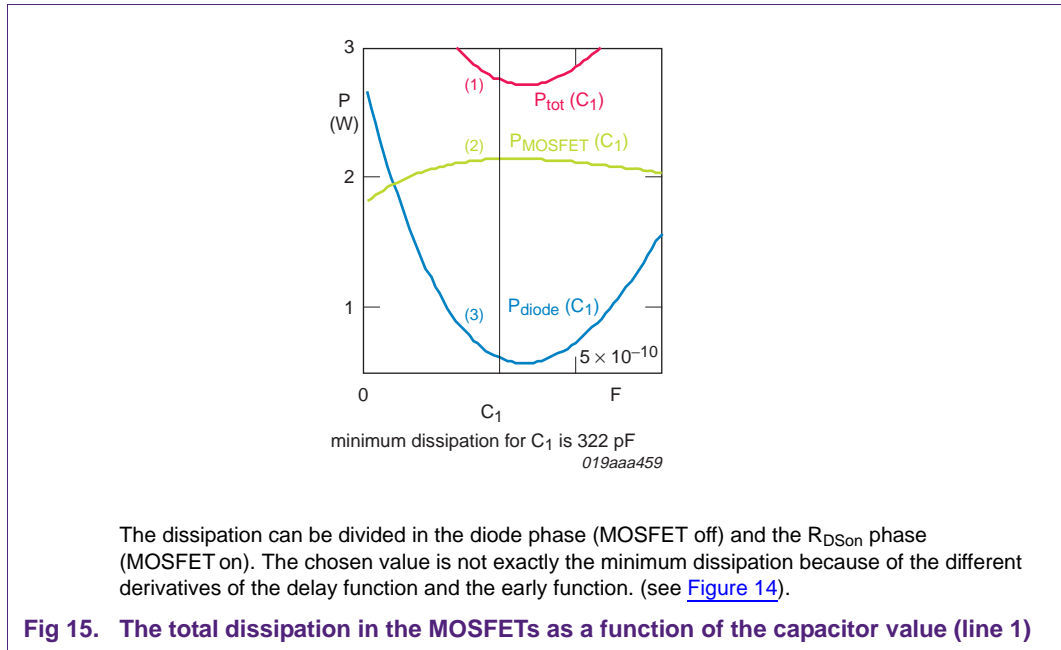
a. Presentation of t_{delay} and t_{till0}-labels in diagram

b. Minimal dissipation when $t_{delay} = t_{till0}$

Fig 14. **The compromise between delay in turn-on time (t_{delay}) and premature turn-off time (t_{till0})**

The calculation of the function $t_{till0} = Early(C_1)$ is explained in Section 11. Here only the result for an amplitude of a current of 34.6 A and a parasitic inductance of 10 nH is given. Figure 15 shows how the total dissipation (P_{tot}) depends on the C_1 value of 322 pF. The minimum dissipation approximately coincides with a C_1 value of 322 pF, where $t_{delay} = t_{till0}$ is valid (see Figure 14). The delay time and the early time are around 510 ns.

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minimum dissipation for C_1 is 322 pF

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The dissipation can be divided in the diode phase (MOSFET off) and the R_{DSon} phase (MOSFET on). The chosen value is not exactly the minimum dissipation because of the different derivatives of the delay function and the early function. (see Figure 14).

Fig 15. The total dissipation in the MOSFETs as a function of the capacitor value (line 1)

In Figure 15 the minimum dissipation does not coincide with the chosen value. This is caused by different values with which the delay function increases and the early function decreases.

The dissipation is increased from 2.171 W (optimal switching) to 2.751 W (with compensation R_1 = 3.9 kΩ, and C_1 = 322 pF). These values are calculated without taking into account the delay in the IC and with a MOSFET used to clamp the filter capacitor voltage to 0 V. If instead of a MOSFET a diode is used, the voltage is clamped to 250 mV.

The new optimal value of C_1 changes to 247.14 pF; t_{delay} = t_{till0} = 726.5 ns); P_{tot} = 3.316 W.

R_1 is dimensioned as R_1 = 3.9 kΩ because the maximum current coming out of the DSA and DSB pins is 1 μA, giving a voltage drop of approximately 4 mV. In the worst case the turn-off threshold level is lowered to −8 mV instead of −12 mV.

The dissipation in the resistor cannot be ignored, because of the relatively low value of R_1 (3.9 kΩ). E.g., when the output voltage is 12 V one of the two resistors will always have a 24 V voltage drop, while the other resistor is at approximately ground level. 24 V means a dissipation of around 150 mW. This can be a problem for very low load specifications. Two options are possible to improve the low load dissipation.

- A switch Q_3 is added in series with R_1 (see Figure 16). The sense is connected to the source of Q_3
- In the second option the source (Q_3) is not connected to the sense input, but the drain (Q_5) is.

Fig 16. Additional switches to decrease the low power losses by adding a circuit
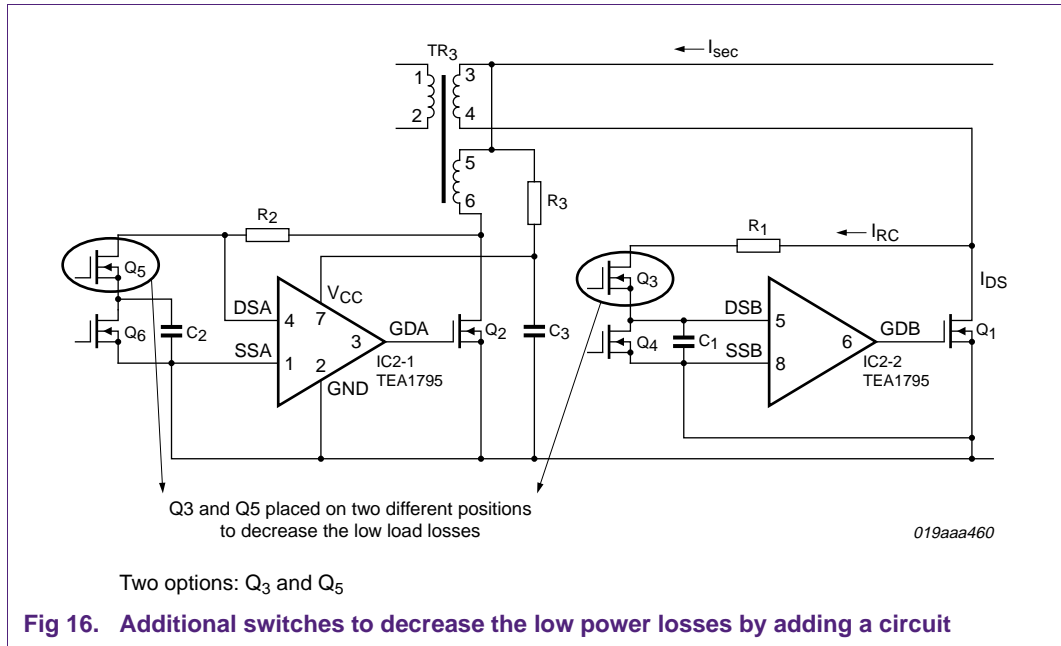
It is important to know how large the compensation capacitor has to be, so the correct MOSFET (Q_3 or Q_5) can be selected. The drain-source capacitance of Q_4 and Q_6 are placed parallel to the compensation capacitance.

Table 2. Compensation capacitance

	V_{DS}		
	100 mV (Typical)	10 V (Typical)	10 V (Maximum)
C_{iss}			
2N7002	41 pF	31 pF	50 pF
BSN20	21 pF	17 pF	27 pF
BSS123	110 pF	55 pF	-
C_{oss}			
2N7002	25 pF	6.8 pF	30 pF
BSN20	17 pF	7 pF	15 pF
BSS123	100 pF	12 pF	-

The timing of the switches (Q_3, Q_4, Q_5, and Q_6) is set in the following way: When the voltage of Q_1 is low, Q_5 has to be off and Q_6 has to be on. On the other hand when the voltage of Q_1 is high Q_5 has to be on and Q_6 has to be off. The same can be said about the state of Q_3 and Q_4 (see Table 3).

Table 3. The states of Q_3, Q_4, Q_5, and Q_6

State	Q_3	Q_4	Q_5	Q_6
Q_1 = LOW; Q_2 = HIGH	off	on	on	off
Q_1 = HIGH; Q_2 = LOW	on	off	off	on

The next step is to find the right driver signals to meet the states in Table 3. There are two options:

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- To derive the signal from the transformer winding
  (see Figure 17, $Q_3 - Q_4$ configuration)

- To derive the signal from the driver output (see Figure 17, $Q_5 - Q_6$ configuration)

If transformer winding is used the gate of Q_3 is connected via a resistance division to the drain of Q_2. Q_4 is connected to the drain of Q_1. The gate of Q_5 is connected to the drain of Q_1 (see Figure 17). The gate of Q_6 is connected to the drain of Q_2.
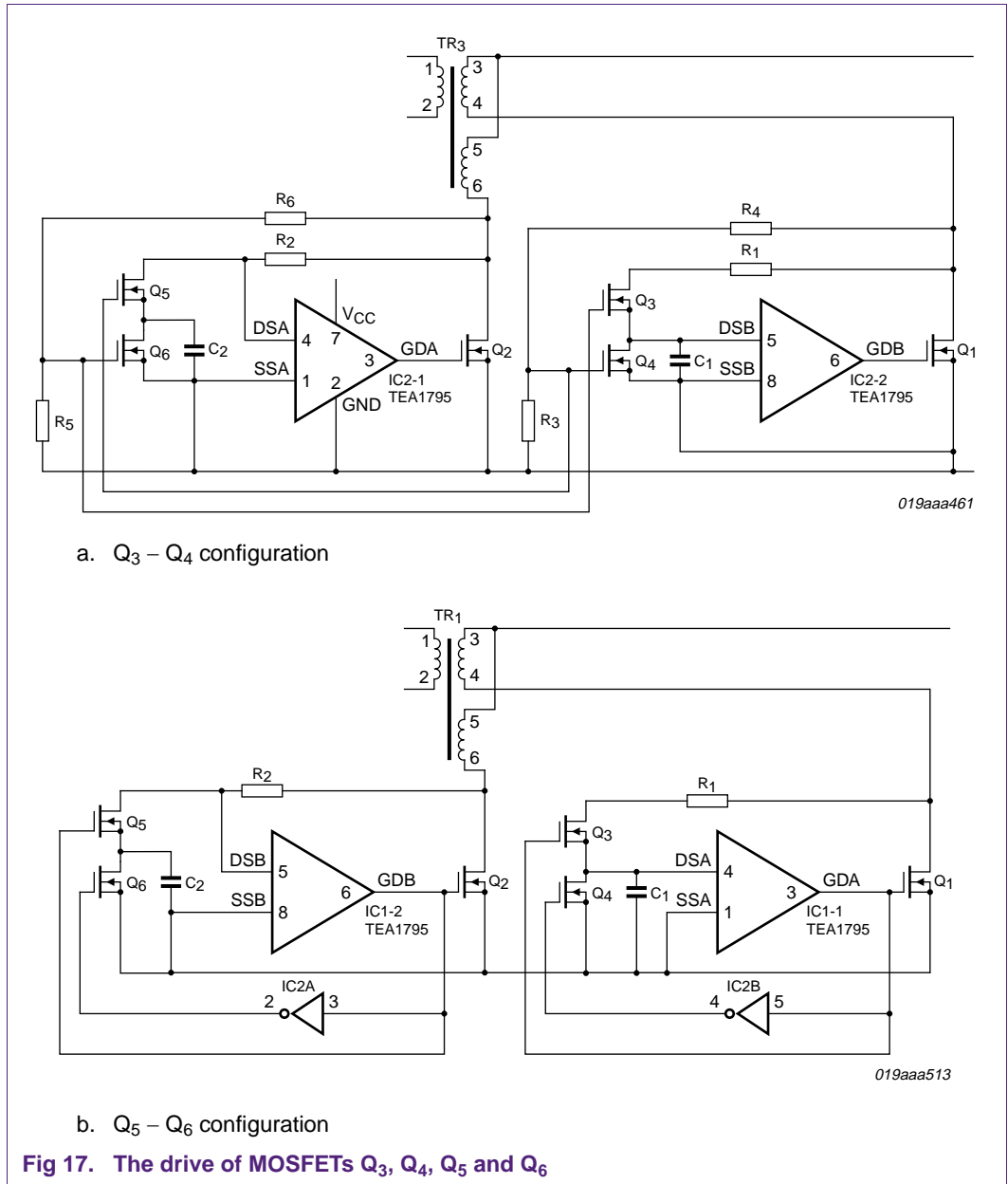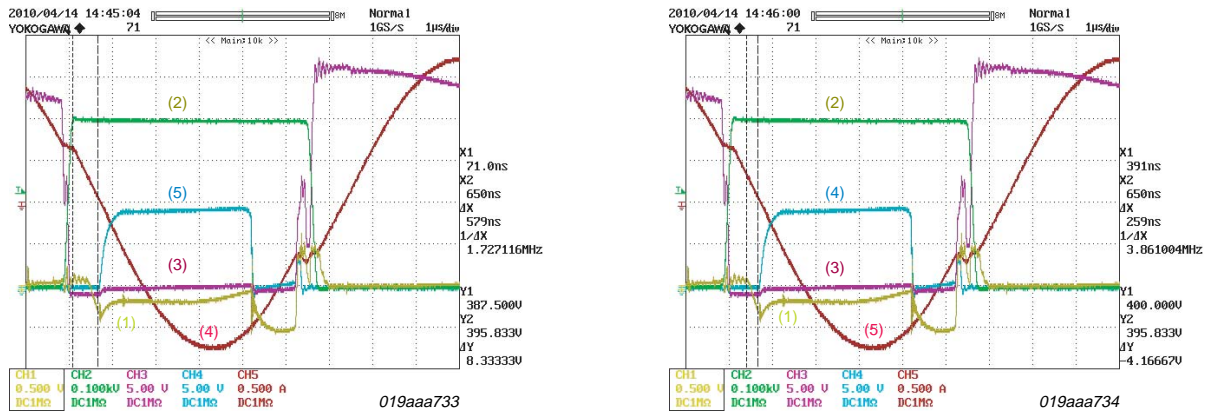
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a. Q$_3$ – Q$_4$ configuration

b. Q$_5$ – Q$_6$ configuration

Fig 17. The drive of MOSFETs Q$_3$, Q$_4$, Q$_5$ and Q$_6$

Figure 18 to Figure 20 show the measurement results for the first schematic ($Q_3 - Q_4$ configuration).

C_1 = 33 pF; R_1 = 3.9 kΩ; I_{load} = 15 A

(1) Voltage on the DSA pin

(2) Half-bridge point

(3) Drain-source voltage on MOSFET

(4) Gate source voltage

(5) Primary transformer current

a. The total delay before MOSFET is turned on (C_1 = 33 pF)

b. The delay caused by the charge of the compensation capacitor (C1 = 33 pF)

Fig 18. Measurement results of the TEA1795 with compensation network

The delay between the current starting to flow through the MOSFET and the turn-on of the MOSFET is 597 ns. 259 ns is caused by charging the capacitor and 338 ns by the delay of switching Q_3 and Q_4. The premature turn-off is approximately 1 μs.
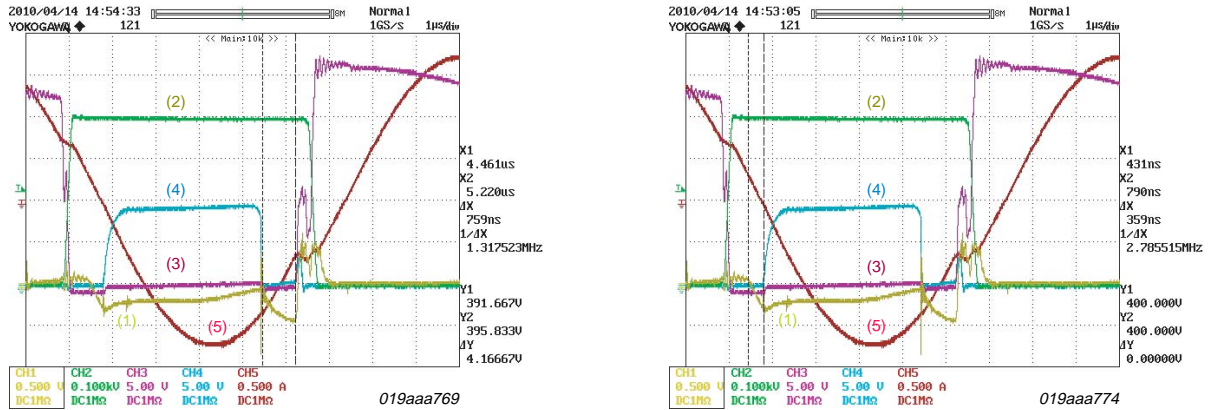
$C_1 = 100$ pF; $R_1 = 3.9$ kΩ; $I_{load} = 15$ A
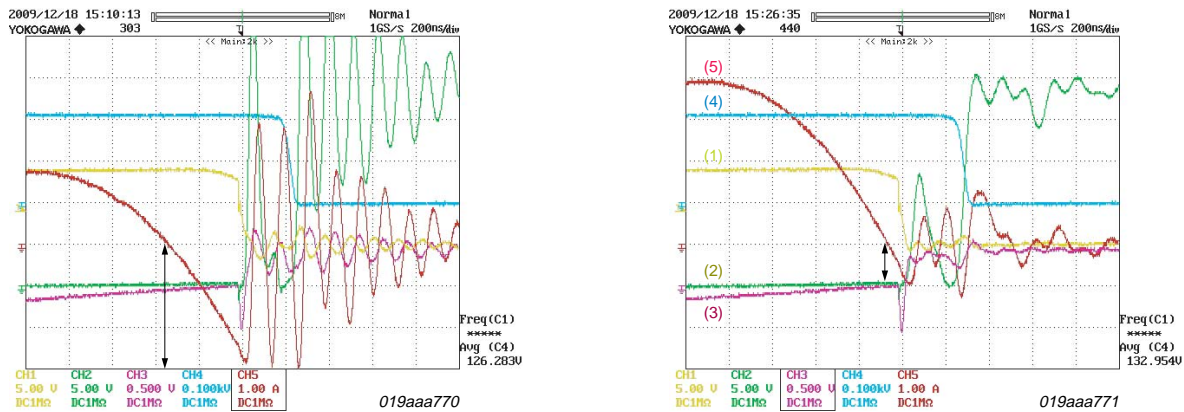
(1) Voltage on the DSA pin

(2) Half-bridge point

(3) Drain-source voltage on MOSFET

(4) Gate source voltage

(5) Primary transformer current

a. The capacitance is increased to 100 pF. The delay is increased with 100 ns (see Figure 18)

b. Increasing the compensation capacitor from 33 pF to 100 pF prematurely causes switching to decrease from 1 μs to 759 ns

Fig 19. Measurement results of the TEA1795 with compensation network

The delay between the current starting to flowing through MOSFET and the turn-on the MOSFET is 697 ns. 359 ns is caused by charging the capacitor and 338 ns is caused by the delay of switching Q_3 and Q_4. The premature turn-off is approximately 759 ns.

8. DCM versus CCM

It does not matter whether the converter is working in CCM mode or DCM mode. There is, however, one exception: the dimensioning of the RC filter is different for DCM and CCM. The MOSFETs have to turn off at the right time to prevent current flowing in the wrong direction (see Figure 20). In Continuous Conductance Mode (CCM) the dI/dt during commutation (going to zero) is much higher than the dI/dt in Discontinuous Conduction Mode (DCM). Therefore, in CCM, the input filter of the IC has to be dimensioned in such a way that only the high frequency oscillation is filtered out and compensation for parasitic inductance is not necessary.

Capacitance = 100 pF; Resistance = 3.9 kΩ; I_{load} = 15 A

(1) Voltage on the DSA pin

(2) Half-bridge point

(3) Drain-source voltage on MOSFET

(4) Gate source voltage

(5) Primary transformer current

a. High reverse current causes a lot of ringing   b. Low reverse current causes much less ringing

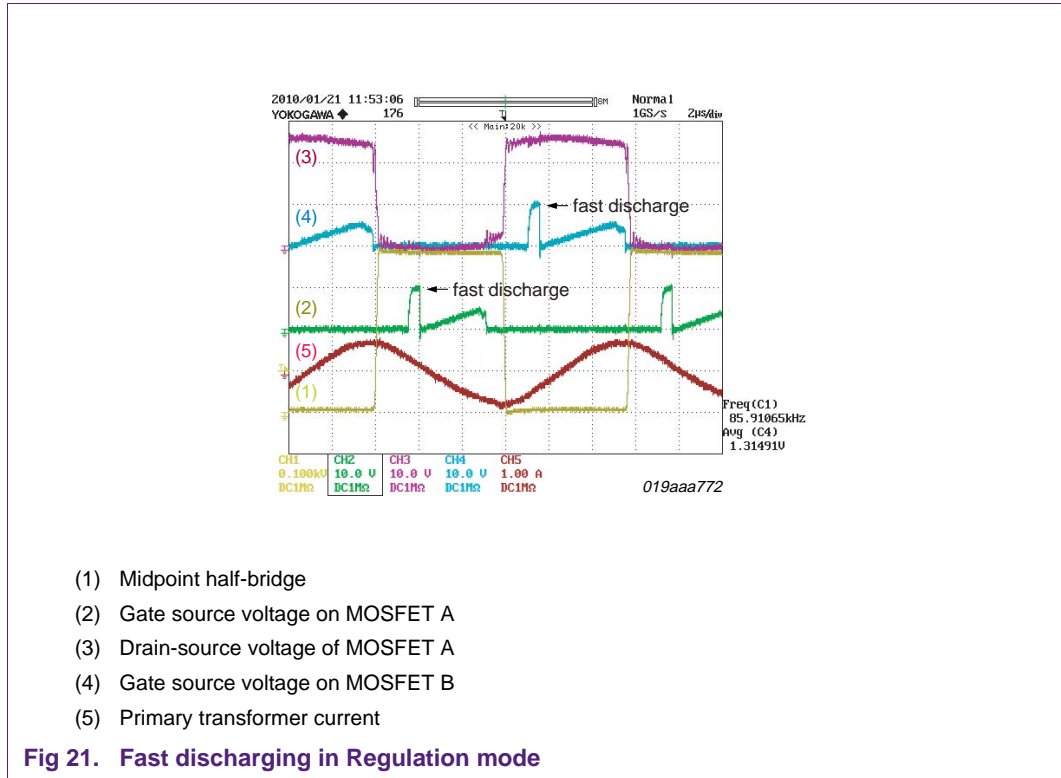**Fig 20. Measurement results of the TEA1795 with compensation network**

9. Issues

9.1 Unstable behavior of the control voltage at low output power

The TEA1795 only turns on the MOSFET if the voltage drop over of the MOSFET is at least 220 mV (see Section 6.1). When the MOSFET is conducting the voltage drops to a few millivolts. This difference in voltage causes a high current dump which again causes a large power transfer per cycle. The transfer can only be changed by changing the control signal. When the voltage drop over of the MOSFET is less than 220 mV no power is delivered to the output. Therefore a small change in the control signal leads to a major difference in power transfer, which causes an oscillation.

9.2 Fast discharging of the gate in Regulation mode

When the blanking time following the turn-on of the SR-MOSFET is passed, the IC changes from On mode to Regulation mode. When the measured drain-source voltage is higher than −25 mV the IC regulates the drain-source voltage to −25 mV. The gate is fully discharged, because the turn-off circuit is also active at that moment. The IC compensates this behavior again by charging the gate voltage. This charge current is only 5 mA so that the charging is very slow. Figure 21 shows the result of this behavior.

(1) Midpoint half-bridge

(2) Gate source voltage on MOSFET A

(3) Drain-source voltage of MOSFET A

(4) Gate source voltage on MOSFET B

(5) Primary transformer current

Fig 21. Fast discharging in Regulation mode

9.3 Power supply in Off mode

If the power supply is in the Off mode, the IC gets no supply. Despite the absence of power the output of the driver is low ohmic. This is caused by an internal charge on a gate of the output MOSFET of the driver. This charge cannot flow away and causes the output of the IC to stay low ohmic. This is important to know when testing the output of the driver.

9.4 Double pulses

It is possible that double pulses on the gate voltage occur. because of the way the SR MOSFETs are controlled (see Figure 22).
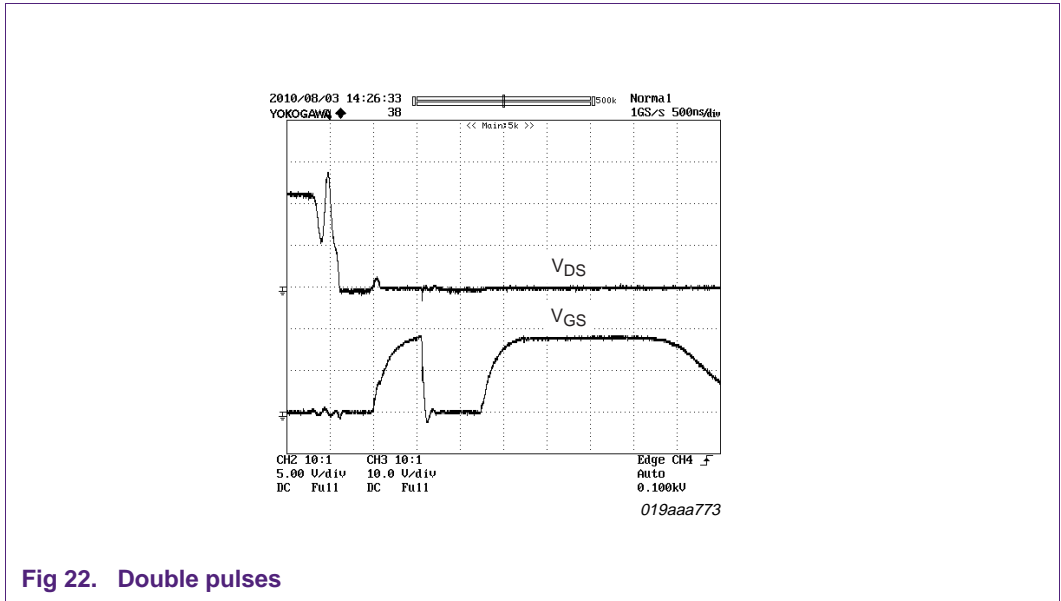
Fig 22. Double pulses

10. Layout of the IC

When designing the layout the following things are important for getting the lowest possible inductance:

- The sense connections must be as close as possible to the pins of the MOSFET
- The loop between the drain sense wire and the source sense wire must be as short as possible
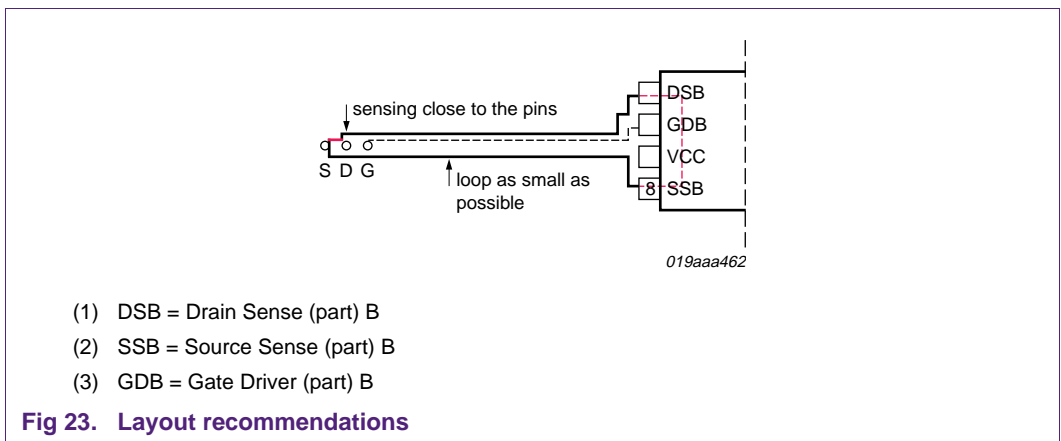
    (1)   DSB = Drain Sense (part) B

    (2)   SSB = Source Sense (part) B

    (3)   GDB = Gate Driver (part) B

Fig 23. Layout recommendations

11. Overview calculations

11.1 DCM mode calculations

Simple presentation of the secondary current:

$$\left[\begin{array}{l} I_{sec} = I_{amp} \times \left| sin(\omega_1 \times (t - k \times t_{no})) \right| \wedge \dfrac{k \times \pi}{\omega_1} \le t \le \dfrac{(k+1) \times \pi}{\omega_1} \wedge k \in N \\[3mm] I_{sec} = 0 \wedge \dfrac{(k+1) \times \pi}{\omega_1} \le t \le \dfrac{(k+1) \times \pi}{\omega_1} + t_{no} \end{array} \right. \tag{19}$$

The switching period can be calculated with Equation 20:

$$t_{sw} = t_{pr} + 2 \times t_{no} = \dfrac{2 \times \pi}{\omega_1} + 2 \times t_{no} \tag{20}$$

P_O the output power, V_O the output voltage, and I_O the output current are related in the following way:

$$P_O = V_O \times I_O \tag{21}$$

A combination of the all equations above results in:

$$P_O = V_O \times \dfrac{1}{\dfrac{\pi}{\omega_1} + t_{no}} \int_0^{\frac{\pi}{\omega_1}} I_{amp} \times sin(\omega_1 \times t) = \dfrac{2}{\pi} \times V_O \times I_{amp} \times \dfrac{\dfrac{2 \times \pi}{\omega_1}}{\dfrac{2 \times \pi}{\omega_1} + t_{no}}$$

$$= \dfrac{2}{\pi} \times V_O \times I_{amp} \times \dfrac{1}{1 + \dfrac{\omega_1 \times t_{no}}{\pi}} \tag{22}$$

The amplitude (I_{amp} in Equation 22) can be calculated with Equation 23:

$$I_{amp} = \left(1 + 2 \times \dfrac{t_{no}}{t_{pr}} \right) \times \dfrac{\pi}{2} \times \dfrac{P_O}{V_O} \tag{23}$$

The average current (I_{avg}) on the secondary side equals the load current, but the RMS current (I_{RMS}) equals:

$$I_{RMS} = \sqrt{ \dfrac{1}{\dfrac{t_{pr}}{2} + t_{no}} \int_0^{\frac{t_{pr}}{2}} I_{amp}^{\;2} \times sin(\omega_1 \times t)^2 } = \dfrac{\pi}{2} \times \dfrac{P_O}{V_O} \times \sqrt{ \dfrac{1}{2} + \dfrac{t_{no}}{t_{pr}} } \tag{24}$$

The voltage drop over the rectifier diode can be calculated with Equation 25:

$$V_f(I_d) = V_{f0} + R_d \times I_d \tag{25}$$

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The dissipation in the two diodes together equals:

$$P = \left(\frac{2}{\pi} \times V_{f0} \times I_{amp} + \frac{1}{2} \times R_d \times I_{amp}^2\right) \times \cfrac{1}{1 + 2 \times \cfrac{t_{no}}{t_{pr}}}$$

$$= \left(V_{f0} \times \frac{P_O}{V_O} + \frac{\pi^2}{8} \times R_d \times \frac{P_O^2}{V_O^2} \times \left(1 + 2 \times \frac{t_{no}}{t_{pr}}\right)\right)$$

(26)

When MOSFETs are used instead of diodes the power dissipation is calculated with Equation 27:

$$P = \frac{1}{2} \times R_{DSon} \times I_{amp}^2 \times \cfrac{1}{1 + 2 \times \cfrac{t_{no}}{t_{pr}}}$$

$$= \frac{\pi^2}{8} \times R_{DSon} \times \frac{P_O^2}{V_O^2} \times \left(1 + 2 \times \frac{t_{no}}{t_{pr}}\right)$$

(27)

If the MOSFETs are switched on too late (t_{delay}) or switched off prematurely (t_{early}), the dissipation can be calculated with Equation 28:

$$P_{loss} = \begin{bmatrix} 2 \times V_f \times I_{amp} \times [2 - [cos(\omega_1 \times t_{delay}) + cos(\omega_1 \times t_{till0})]] + \\[2mm] \begin{bmatrix} I_{amp}^2 \times \omega_1 \times (t_{delay} + t_{till0}) \times (R_d - R_{DSon}) - \\[1mm] \frac{1}{2} \times (R_d - R_{DSon}) \times I_{amp}^2 \times (sin(2 \times \omega_1 \times t_{delay}) + sin(2 \times \omega_1 \times t_{till0})) + \end{bmatrix} \\[4mm] R_{DSon} \times I_{amp}^2 \times (\pi) \end{bmatrix}$$

$$\times \frac{1}{\pi + t_{on} \times \omega_1}$$
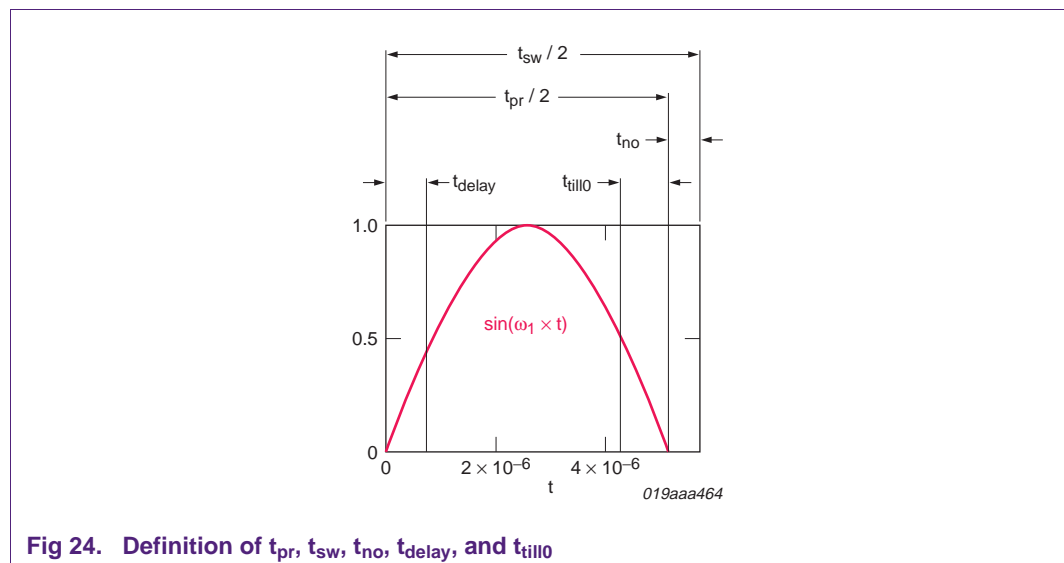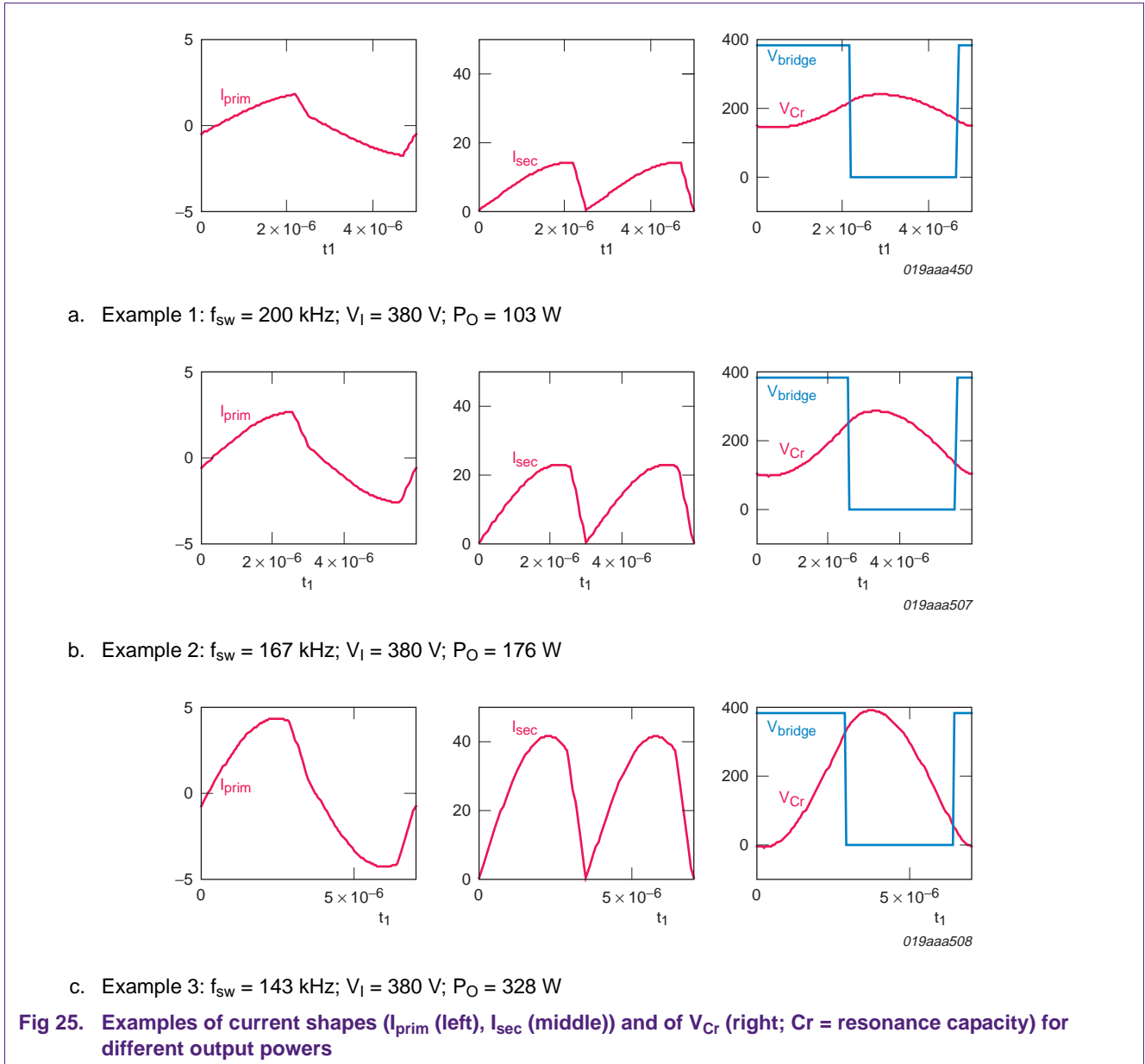
(28)

Fig 24. Definition of t_{pr}, t_{sw}, t_{no}, t_{delay}, and t_{till0}

11.2 CCM mode calculations

In case of CCM the secondary current has a slightly different shape. Figure 25 shows three examples:

a. Example 1: f_{sw} = 200 kHz; V_I = 380 V; P_O = 103 W

b. Example 2: f_{sw} = 167 kHz; V_I = 380 V; P_O = 176 W

c. Example 3: f_{sw} = 143 kHz; V_I = 380 V; P_O = 328 W

Fig 25. Examples of current shapes (I_{prim} (left), I_{sec} (middle)) and of V_{Cr} (right; Cr = resonance capacity) for different output powers

The secondary current can be approximated with Equation 29:

$$I_{sec} = I_{amp} \times \left| sin(\omega_1 \times (t + k \times t_{till0})) \right| \wedge k \times \frac{\pi}{\omega_1} \leq t < (k+1) \times \left(\frac{\pi}{\omega_1} - t_{till0} \right) \wedge k \in N \qquad (29)$$
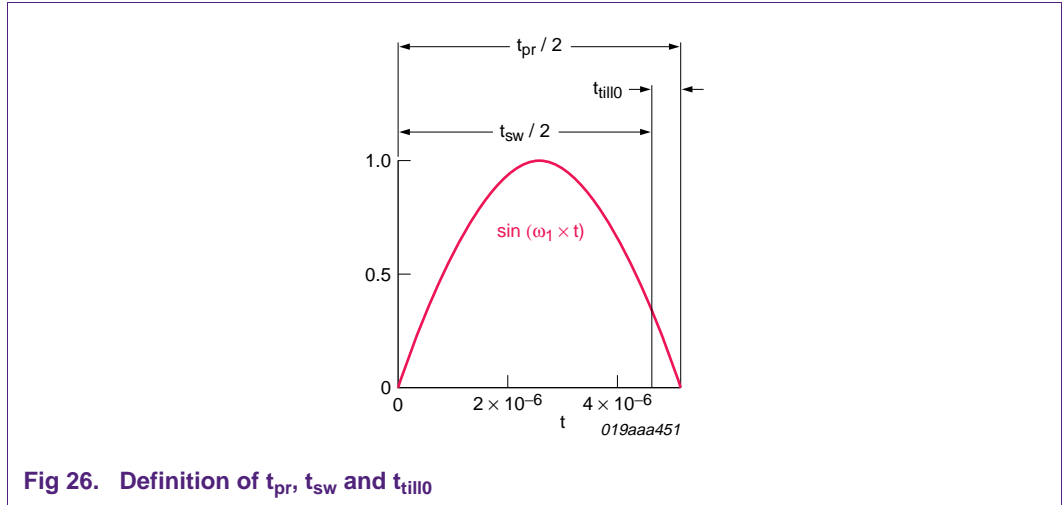
Fig 26. Definition of t_{pr}, t_{sw} and t_{till0}

See Figure 26 for the definition of the variables t_{sw}, t_{pr} and t_{till0}.

The equivalent to the DCM case P_O can be written as Equation 30:

$$
\begin{aligned}
P_O &= V_O \times \frac{2}{\frac{t_{pr}}{2} - t_{till0}} \times \int_{0}^{\left(\frac{t_{pr}}{2} - t_{till0}\right)} I_{amp} \times sin(\omega_1 \times t) \times dt \\[2em]
&= \frac{2}{\pi} \times V_O \times I_{amp} \times \frac{1 - cos\left(\pi \times \left(1 - \frac{2 \times t_{till0}}{t_{pr}}\right)\right)}{2 \times \left(1 - \frac{2 \times t_{till0}}{t_{pr}}\right)}
\end{aligned}
\tag{30}
$$

For a given P_O and V_O this expression can be rewritten as Equation 31:

$$
I_{amp} = \frac{\pi}{2} \times \frac{P_O}{V_O} \times \frac{2 \times \left(1 - \frac{2 \times t_{till0}}{t_{pr}}\right)}{1 - cos\left(\pi \times \left(1 - \frac{2 \times t_{till0}}{t_{pr}}\right)\right)}
\tag{31}
$$

Equation 31 is the expression for the effective current.

$$
I_{RMS}(t_{till0}) = \sqrt{\frac{1}{2}} \times \frac{P_O}{V_O} \times \frac{\pi}{2} \times \frac{2 \times \left(1 - \frac{2 \times t_{till0}}{t_{pr}}\right)}{1 - cos\left[\pi \times \left(1 - \frac{2 \times t_{till0}}{t_{pr}}\right)\right]} \times
$$

$$
\sqrt{1 - \left[\frac{sin\left[2 \times \pi \times \left(1 - \frac{2 \times t_{till0}}{t_{pr}}\right)\right]}{2 \times \pi \times \left(1 - \frac{2 \times t_{till0}}{t_{pr}}\right)}\right]}
\tag{32}
$$

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The voltage drop over the rectifier diode can be calculated with Equation 33:

$$V_f(I_d) \;=\; V_{f0} + R_d \times I_d \tag{33}$$

The dissipation in the two diodes together equals:

$$P \;=\; V_{f0} \times \frac{P_O}{V_O} + \frac{1}{2} \times R_d \times \frac{P_O^{\,2}}{V_O^{\,2}} \times \frac{\pi^2 \times \left(1 - \dfrac{2 \times t_{till0}}{t_{pr}}\right)}{\left(1 - cos\left(\pi \times \left(1 - \dfrac{2 \times t_{till0}}{t_{pr}}\right)\right)\right)^2} \times$$

$$\left(1 - \frac{sin\left(2 \times \pi \times \left(1 - \dfrac{2 \times t_{till0}}{t_{pr}}\right)\right)}{2 \times \pi \times \left(1 - \dfrac{2 \times t_{till0}}{t_{pr}}\right)}\right) \tag{34}$$

Example:

- t_{pr} = 11 μs
- t_{till0} = 500 ns
- P_O = 240 W
- V_O = 12 V
- R_d = 5 mΩ
- V_{f0} = 280 mV

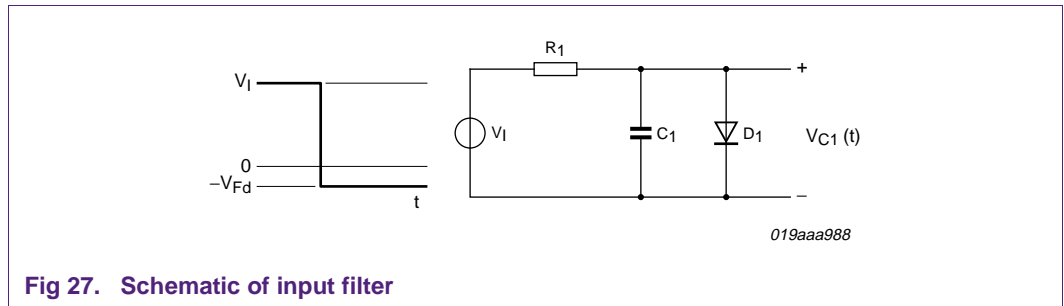The dissipation in the diodes equals: 7.925 W.

11.3 Input filter

Fig 27. Schematic of input filter

The output voltage of the input filter shown in Figure 27 can be calculated with Equation 35:

$$V_{C1}(t) \;=\; V_{C10} \times exp\left(-\frac{t}{R_1 \times C_1}\right) + V_I \times \left(1 - exp\left(-\frac{t}{R_1 \times C_1}\right)\right) \tag{35}$$

Where:

- V_{C1} = voltage on capacitor C_1
- V_{C10} = boundary condition of the capacitor voltage
- V_I = input voltage

With Equation 35 t_{delay} can be calculated.

When:

- $V_{C10} = V_{F(D1)}$ (forward voltage of diode D_1)
- $V_I = V_{F(MOSFET)}$ (diode of MOSFET Q_1 or Q_2) (see Figure 11)
- $t = t_d$
- $V_{C1} = V_{th}$ (−220 mV)

Equation 35 changes to Equation 36:

$$V_{CI}(t_d) = V_{F(D1)} \times exp\left(-\frac{t_d}{R_1 \times C_I}\right) + V_{F(MOSFET)} \times \left(1 - exp\left(-\frac{t_d}{R_1 \times C_I}\right)\right) = V_{th} \tag{36}$$

Then t_{delay} can be calculated with Equation 37

$$t_d = -R_1 \times C_I \times \ln\left(-\frac{(V_{th} - V_{F(MOSFET)})}{(V_{F(D1)} - V_{F(MOSFET)})}\right) \tag{37}$$

11.4 Parasitic inductance

$$V_L(t) = L_{par} \times \frac{di_{ds}}{dt} \tag{38}$$

If the secondary current can be calculated with Equation 39:

$$I_{DS}(t) = I_{amp} \times sin(\omega_I \times t) \tag{39}$$

then the induced voltage becomes:

$$V_L(t) = L_{par} \times \frac{d(I_{amp} \times sin(\omega_I \times t))}{dt} = I_{amp} \times L_{par} \times \omega_I \times cos(\omega_I \times \varphi) \tag{40}$$

The total voltage measured equals:

$$\begin{bmatrix} V_{DS}(t) = I_{amp} \times L_{par} \times \omega_I \times cos(\omega_I \times t) + R_{DSon} \times I_{amp} \times sin(\omega_I \times t) \\ \quad = I_{amp} \times \sqrt{(L_{par}^2 \times \omega_I^2 + R_{DSon}^2)} \times cos(\omega_I \times t - \varphi) \\ \varphi = atan\left(\frac{R_{DSon}}{L_{par} \times \omega_I}\right) \end{bmatrix} \tag{41}$$

Finally, the premature turn-off time equals t_1 in:

$$\frac{t_{pr}}{2} - t_1 = acos\left(\frac{V_{th}}{I_{amp} \times \sqrt{L_{par}^2 \times \omega_I^2 + R_{DSon}^2}}\right) + \varphi \tag{42}$$

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11.5 Compensation filter

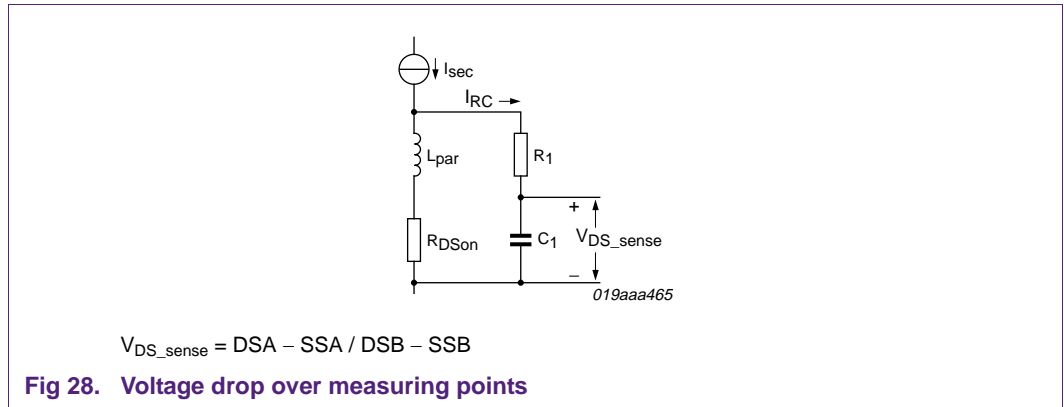$$\begin{bmatrix} I_{\text{sec}}(s) = I_{ds}(s) + I_{RC}(s) \\ R_1 \times I_{RC} + V_{C1} = L_{par} \times \dfrac{di_{ds}}{dt} + R_{DSon} \times I_{DS} \\ I_{RC} = C_1 \times \dfrac{du_{C1}}{dt} \end{bmatrix} \tag{43}$$

$$\frac{L_{par}}{R_{DSon}} = R_1 \times C_1 \tag{44}$$

$$V_{C1} = R_{DSon} \times I_{ds} \tag{45}$$

The voltage drop over the measuring points caused by the parasitic inductance equals:

$$V_{DS}(t) = L_{par} \times \frac{di_{\text{sec}}}{dt} + R_{DSon} \times I_{\text{sec}} \tag{46}$$

$$V_{DS\_sense} = DSA - SSA / DSB - SSB$$

Fig 28. Voltage drop over measuring points

$$\begin{bmatrix} I_{\text{sec}} = I_{DS} + I_{RC} \\ R_1 \times I_{RC} + V_{C1} = L_{par} \times \dfrac{di_{ds}}{dt} + R_{DSon} \times I_{ds} \\ I_{RC} = C_1 \times \dfrac{du_{C1}}{dt} \\ V_{C1} = V_{DS\_sense} \end{bmatrix} \Rightarrow$$

$$\begin{bmatrix} R_1 \times I_{RC} + V_{DS\_sense} = L_{par} \times \dfrac{d(I_{\text{sec}} - I_{RC})}{dt} + R_{DSon} \times (I_{\text{sec}} - I_{RC}) \\ I_{RC} = C_1 \times \dfrac{du_{ds\_sense}}{dt} \end{bmatrix} \Rightarrow \tag{47}$$

$$\left[R_1 \times C_1 \times \frac{du_{ds\_sense}}{dt} + V_{DS\_sense} = L_{par} \times \frac{d(I_{\text{sec}} - I_{RC})}{dt} + R_{DSon} \times \left(I_{\text{sec}} - C_1 \times \frac{du_{ds\_sense}}{dt} \right) \right.$$

Laplace transformation

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$$(R_1 + R_{DSon}) \times C_1 \times \frac{du_{\text{ds\_sense}}}{dt} + V_{DS\_\text{sense}} = L_{par} \times \frac{d(I_{\text{sec}} - I_{RC})}{dt} + R_{DSon} \times I_{\text{sec}} \Rightarrow$$

$$(R_1 + R_{DSon}) \times C_1 \times s \times V_{DS\_\text{sense}} + V_{DS\_\text{sense}} = L_{par} \times s \times I_{DS} - s \times I_{RC} + R_{DSon} \times I_{\text{sec}} \Rightarrow$$

$$V_{DS\_\text{sense}} = I_{\text{sec}} \times R_{DSon} \times \left(\frac{\frac{L_{par}}{R_{DSon}} \times s + 1}{(R_1 + R_{DSon}) \times C_1 \times s + 1} \right) - \frac{s \times I_{RC}}{(R_1 + R_{DSon}) \times C_1 \times s + 1}$$

(48)

If the first term:

$$\frac{\frac{L_{par}}{R_{DSon}} \times s + 1}{(R_1 + R_{DSon}) \times C_1 \times s + 1} = 1$$

(49)

and the second term:

$$\frac{s \times I_{RC}}{(R_1 + R_{DSon}) \times C_1 \times s + 1}$$
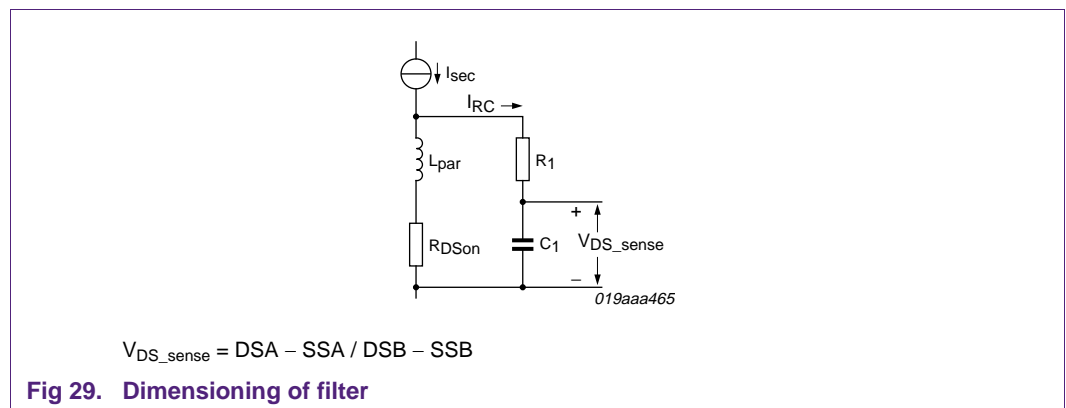
(50)

are negligible, then:

$$V_{DS\_\text{sense}} = I_{\text{sec}} \times R_{DSon}$$

(51)

The first term equals 1 if is valid:

$$\frac{\frac{L_{par}}{R_{DSon}} \times s + 1}{(R_1 + R_{DSon}) \times C_1 \times s + 1} = 1 \Rightarrow \frac{L_{par}}{R_{DSon}} = (R_1 + R_{DSon}) \times C_1 \Rightarrow$$

$$C_1 = \frac{L_{par}}{R_{DSon} \times (R_1 + R_{DSon})}$$

(52)

The second term is small because I_{RC} is small.

11.6 Dimensioning of filter

$$V_{DS\_\text{sense}} = DSA - SSA / DSB - SSB$$

Fig 29. Dimensioning of filter

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$$I_{\text{sec}} = A \times sin(\omega_1 \times t + \varphi) = A \times (cos(\varphi) \times sin(\omega_1 \times t) + sin(\varphi) \times cos(\omega_t \times t)) \xrightarrow{s}$$

$$A \times \frac{cos(\varphi) \times \omega_1 + sin(\varphi) \times s}{s^2 + \omega_1^2} \tag{53}$$

$$\begin{cases} I_{\text{sec}} = I_{DS} + I_{RC} \\ R_1 \times I_{RC} + V_{C1} = L_{par} \times \dfrac{di_{ds}}{dt} + R_{DSon} \times I_{DS} \\ I_{RC} = C_1 \times \dfrac{du_{C1}}{dt} = \\ V_{C1} = V_{\text{ds\_sense}} \end{cases} \Rightarrow \begin{cases} L_{par} \times \dfrac{di_{ds}}{dt} = -(R_{DSon} + R_1) \times I_{DS} + R_1 \times I_{\text{sec}} \\ + u_{C1} \\ C_1 \times \dfrac{du_{C1}}{dt} = I_{\text{sec}} - I_{DS} \end{cases}$$

$$\Rightarrow \begin{pmatrix} \dfrac{di_{ds}}{dt} \\ \dfrac{du_{C1}}{dt} \end{pmatrix} = \begin{pmatrix} L_{par} & 0 \\ 0 & C_1 \end{pmatrix}^{-1} \times \begin{pmatrix} -(R_{DSon} + R_1) & +1 \\ -1 & 0 \end{pmatrix} \times \begin{pmatrix} I_{DS} \\ V_{C1} \end{pmatrix} + \begin{pmatrix} L_{par} & 0 \\ 0 & C_1 \end{pmatrix}^{-1} \tag{54}$$

$$\times \begin{pmatrix} R_1 & 0 \\ 1 & 0 \end{pmatrix} \times \begin{pmatrix} I_{\text{sec}} \\ 0 \end{pmatrix} \Rightarrow A \times \begin{pmatrix} \dfrac{di_{ds}}{dt} \\ \dfrac{du_{C1}}{dt} \end{pmatrix} = A_{mat} \times \begin{pmatrix} I_{DS} \\ V_{C1} \end{pmatrix} + B_{mat} \times \begin{pmatrix} I_{\text{sec}} \\ 0 \end{pmatrix}$$

$$A_{mat} = \begin{pmatrix} L_{par} & 0 \\ 0 & C_1 \end{pmatrix}^{-1} \times \begin{pmatrix} R_{DSon} + R_1 & -1 \\ -1 & 0 \end{pmatrix} \tag{55}$$

$$B_{mat} = \begin{pmatrix} L_{par} & 0 \\ 0 & C_1 \end{pmatrix}^{-1} \times \begin{pmatrix} -R_1 & 0 \\ 1 & 0 \end{pmatrix} \tag{56}$$

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with Laplace transformation and T-matrix with eigenvectors.

$$\left.\begin{array}{r}\dot{x} = A_{mat} \times x + B_{mat} \times \begin{pmatrix} I_{\sec} \\ 0 \end{pmatrix} \\ x = T \times y \end{array}\right\} \Rightarrow T \times \dot{y} = A_{mat} \times T \times y + B_{mat} \times \begin{pmatrix} I_{\sec} \\ 0 \end{pmatrix} \Rightarrow$$

$$\left.\dot{y} = T^{-1} \times A_{mat} \times T \times y + T^{-1} \times B_{mat} \times \begin{pmatrix} I_{\sec} \\ 0 \end{pmatrix}\right\} \Rightarrow$$

$$\Lambda = T^{-1} \times A_{mat} \times T \Rightarrow$$

$$\dot{y} = \Lambda \times y + T^{-1} \times B_{mat} \times \begin{pmatrix} I_{\sec} \\ 0 \end{pmatrix} \overset{s-domain}{\rightarrow} \tag{57}$$

$$(s \times I - \Lambda) \times y = y_0 + T^{-1} \times B_{mat} \times \begin{pmatrix} I_{\sec}(s) \\ 0 \end{pmatrix} \Rightarrow$$

$$y = (s \times I - \Lambda)^{-1} \times y_0 + (s \times I - \Lambda)^{-1} \times \frac{\cos(\varphi) \times \omega_1 + \sin(\varphi) \times s}{s^2 + \omega_1^2} \times T^{-1} \times B_{mat} \times \begin{pmatrix} I_{\sec} \\ 0 \end{pmatrix} \Rightarrow$$

$$x = T \times (s \times I - \Lambda)^{-1} \times T^{-1} \times x_0 + (s \times I - \Lambda)^{-1} \times \frac{\cos(\varphi) \times \omega_1 + \sin(\varphi) \times s}{s^2 + \omega_1^2} \times T^{-1} \times B_{mat} \times \begin{pmatrix} I_{\sec} \\ 0 \end{pmatrix}$$

$$x = T \times (sI - \Lambda)^{-1} \times T^{-1} \times x_0 + T \times (sI - \Lambda)^{-1} \times \frac{\cos(\varphi) \times \omega_1 + \sin(\varphi) \times s}{s^2 + \omega_1^2}$$

$$\times T^{-1} \times B_{mat} \times \begin{pmatrix} A \\ 0 \end{pmatrix} \overset{timedomain}{\rightarrow} \tag{58}$$

$$x(t) = T \times exp(t) \times T^{-1} \times x_0 + T \times exp2(t) \times T^{-1} \times B_{mat} \times \begin{pmatrix} A \\ 0 \end{pmatrix}$$

Where:

- x_0 = The boundary conditions
- p_1 and p_2 = The poles of the system
- T = the eigenvectors of the system
- I = the identity matrix

$$exp(t) = \begin{pmatrix} exp(p_1 \times t) & 0 \\ 0 & exp(p_2 \times t) \end{pmatrix} \tag{59}$$

$$exp2(t) = \begin{pmatrix} f_1(t) & 0 \\ 0 & f_2(t) \end{pmatrix} \tag{60}$$

$$f_1(t) = \frac{\omega_1 \times \cos(\varphi) + p_1 \times \sin(\varphi)}{\omega_1^2 + p_1^2} \times (exp(p_1 \times t) - \cos(\omega_1 \times t)) +$$

$$\frac{\omega_1 \times \sin(\varphi) - p_2 \times \cos(\varphi)}{\omega_1^2 + p_1^2} \times \sin(\omega_1 \times t) \times T \tag{61}$$

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$$f_2(t) = \frac{\omega_1 \times cos(\varphi) + P_2 \times sin(\varphi)}{\omega_1^2 + P_2^2} \times (exp(p_1 \times t) - cos(\omega_1 \times t)) +$$

$$\frac{\omega_1 \times sin(\varphi) - P_2 \times cos(\varphi)}{\omega_1^2 + P_2^2} \times sin(\omega_1 \times t)$$

(62)

With $t_{delay} = -RC \times 1n \times \left(\frac{V_{th} - V_I}{V_{DS0} - V_I}\right)$ φ can be calculated: $\varphi = \omega_1 \times t_{delay}$.

If t_1 is the time V_c (t_1) = V_{th} and t_{pr} is the period time of secondary current then $t_{till0} = t_{pr} - t_1$.

The best choice for the capacitor value is when $t_{delay} = t_{till0}$

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